

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M SFF core logic

SKYY

2008-07-29

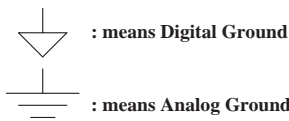
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	SCHEMATIC, M/B LA-4021P
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Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+B	+5VALW +3VALW +3VM +1.05VM	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +0.9V
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



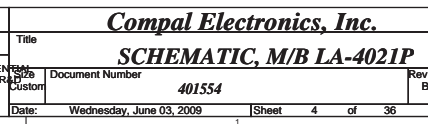
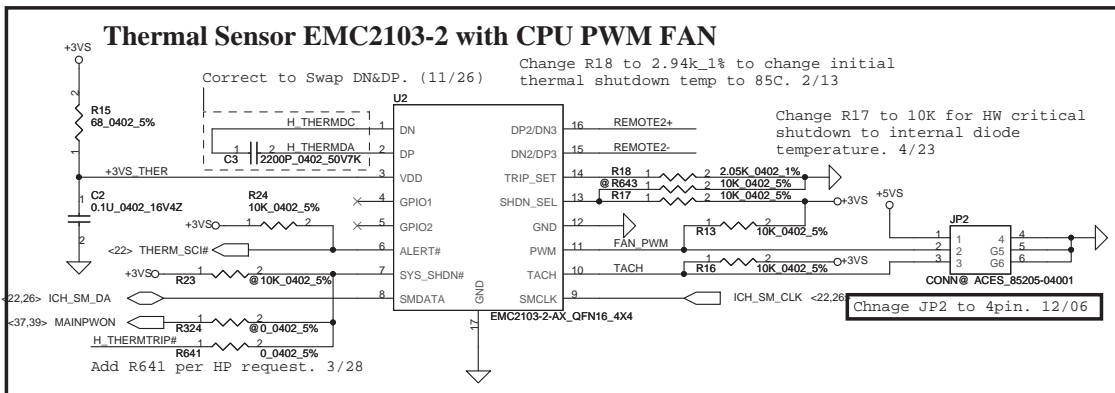
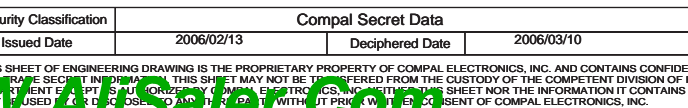
@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

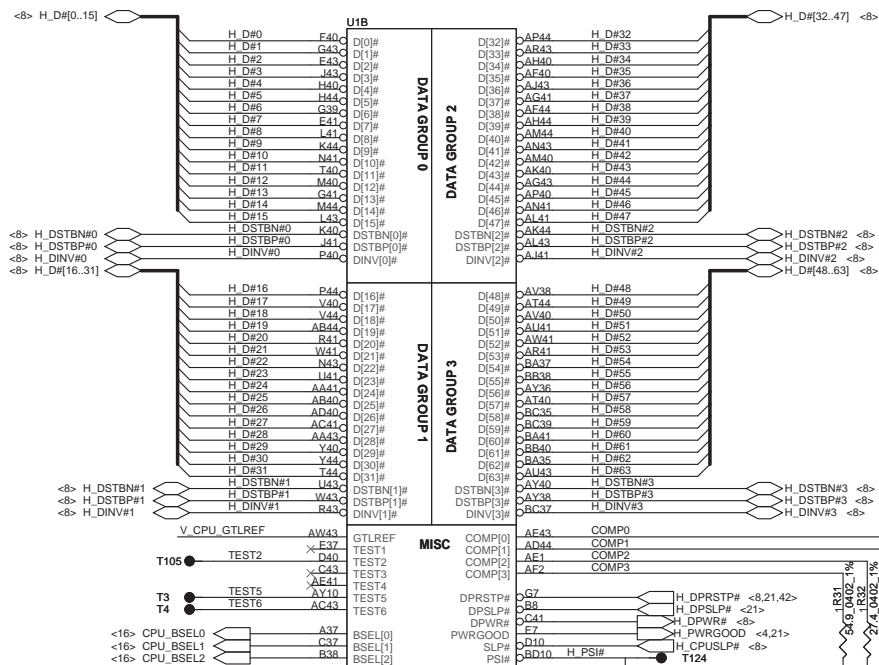
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0



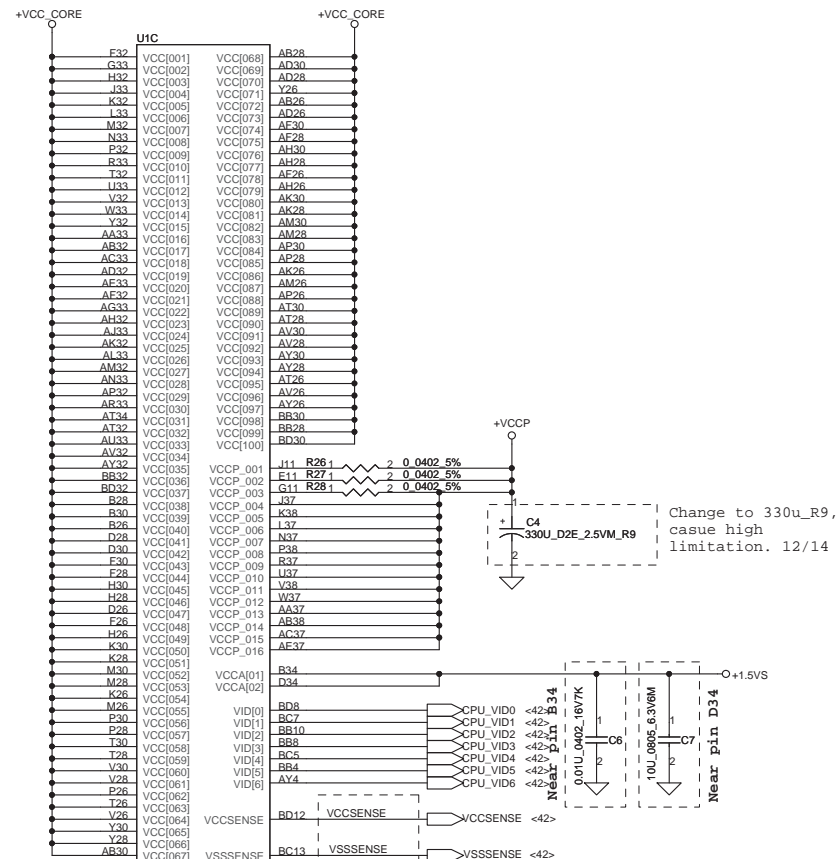
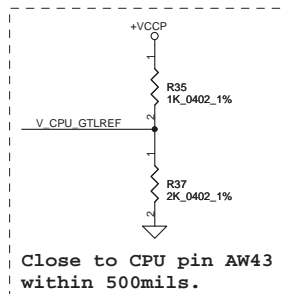


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TFS

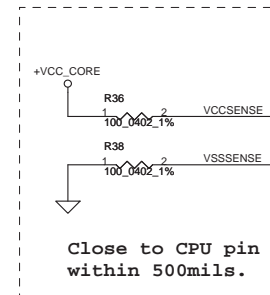
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

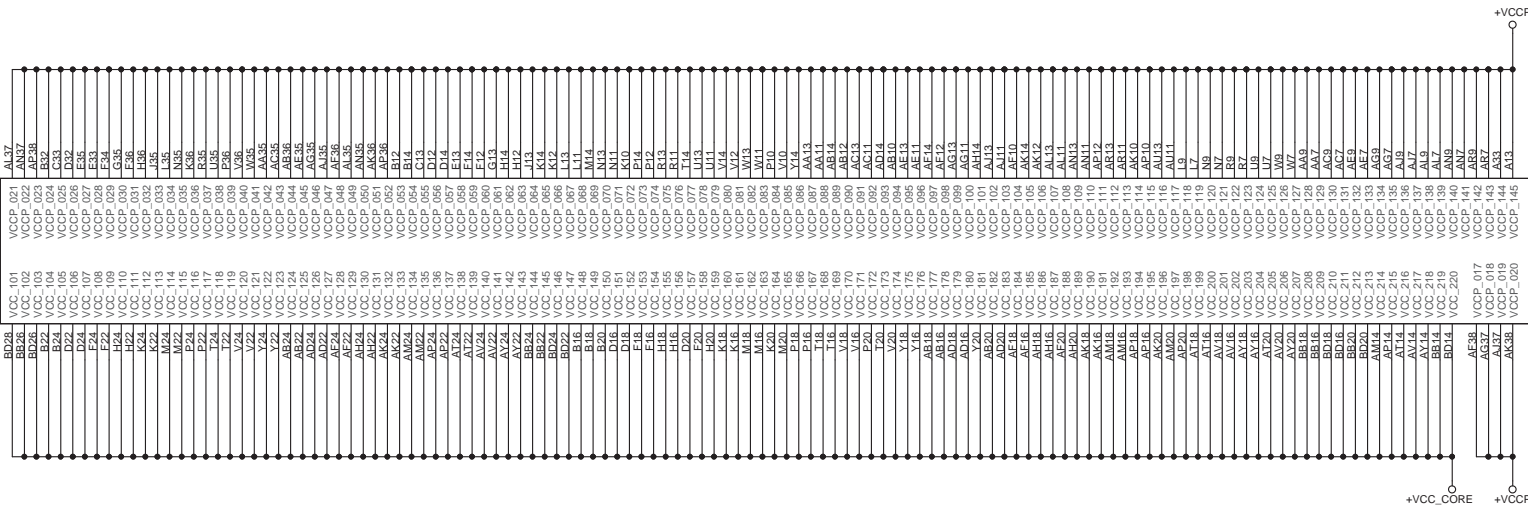
Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



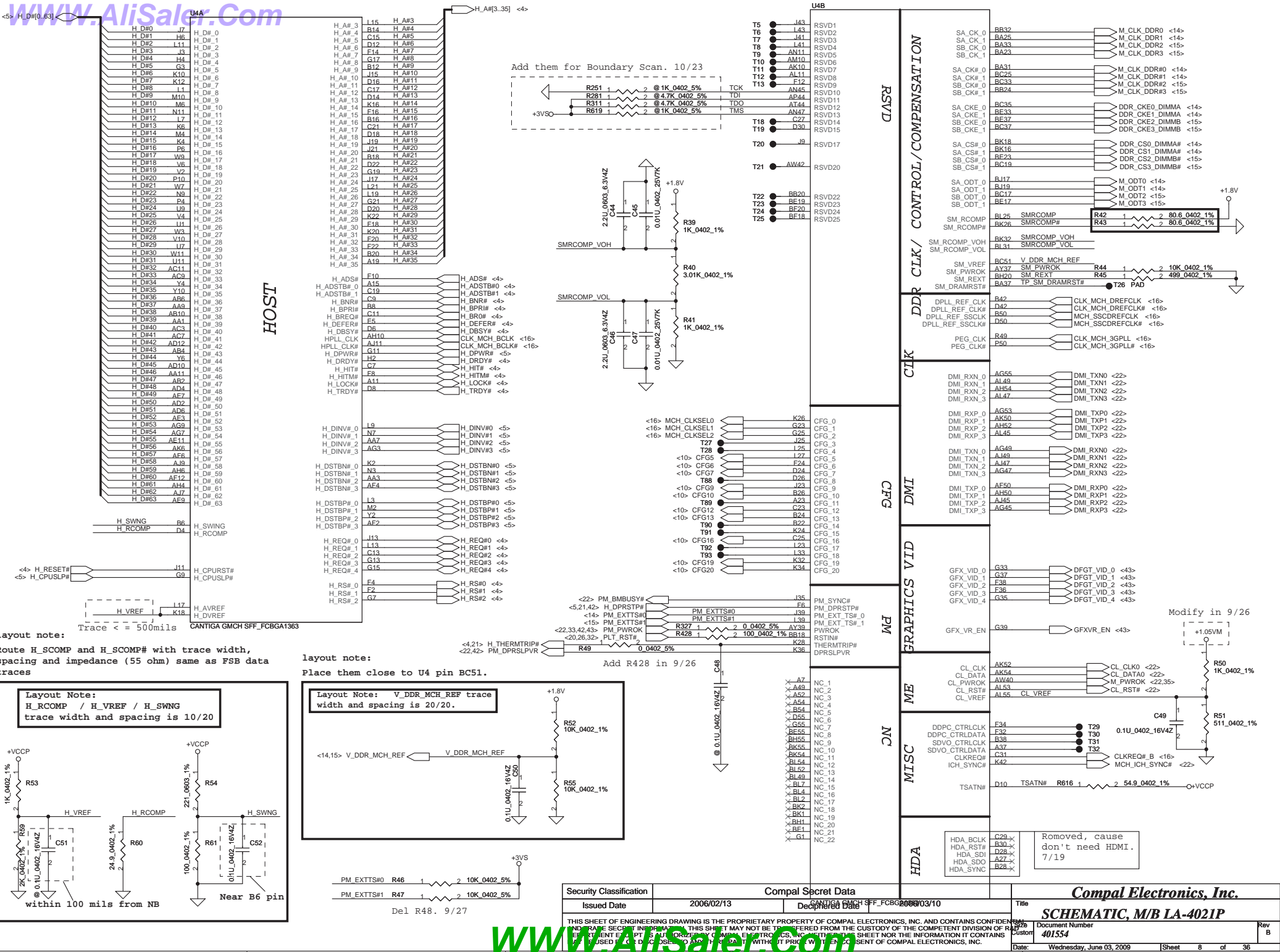
Length match within 25 mils. The trace width/space/other is 20/7/25.

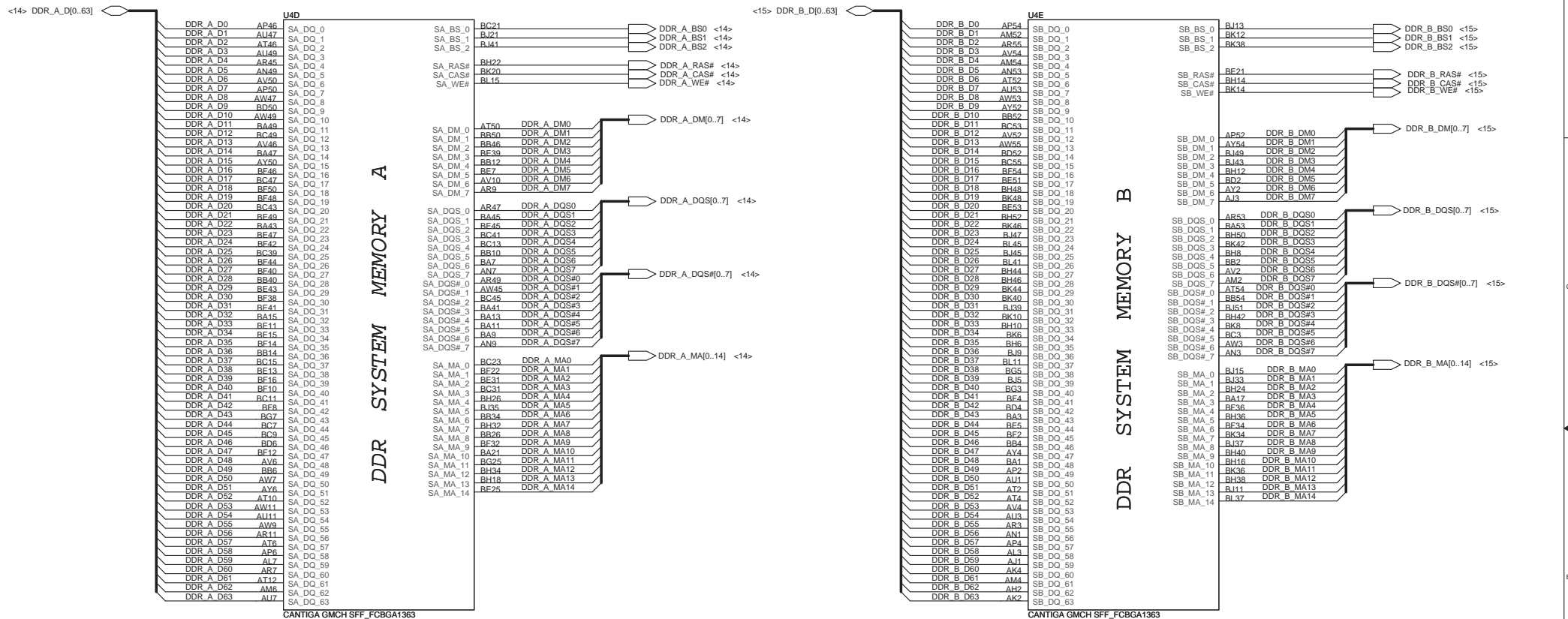


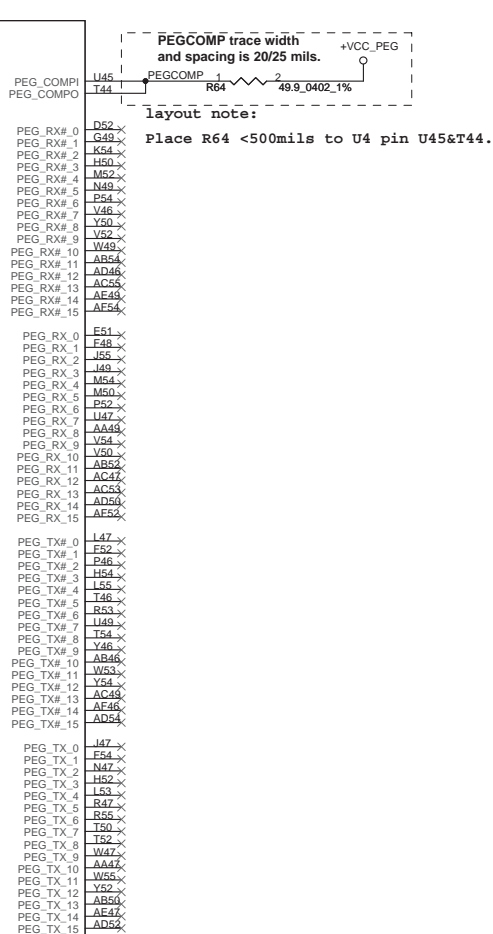
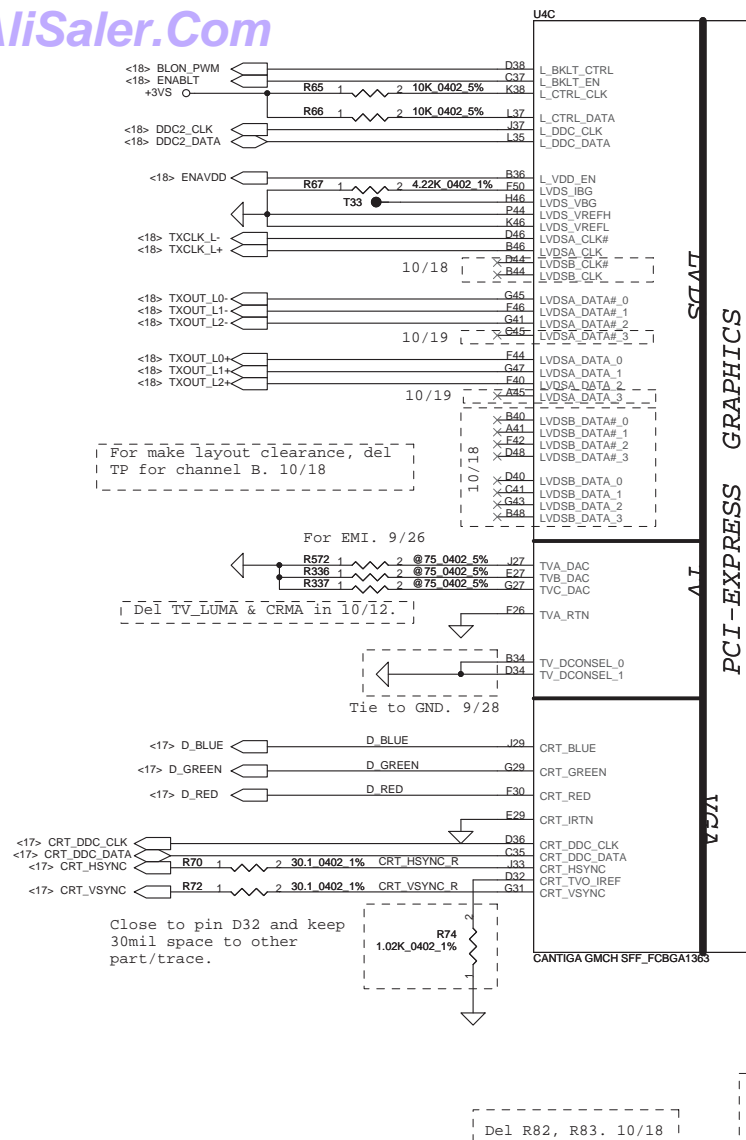


U1F
PENRYN SFF_UFCBGA956

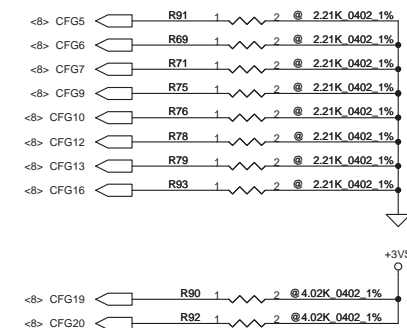
U1D	U1E
B42	VSS1001
F44	VSS1002
D44	VSS1003
D42	VSS1004
F42	VSS1005
H42	VSS1006
K42	VSS1007
M42	VSS1008
P42	VSS1009
T42	VSS1010
Y42	VSS1011
AB42	VSS1012
AD42	VSS1013
AF42	VSS1014
AH42	VSS1015
AK42	VSS1016
AM42	VSS1017
AP42	VSS1018
AV44	VSS1019
AV44	VSS1020
AT42	VSS1021
AV42	VSS1022
AY42	VSS1023
BA43	VSS1024
BB42	VSS1025
CB42	VSS1026
CC42	VSS1027
CD42	VSS1028
CE42	VSS1029
CF42	VSS1030
CG42	VSS1031
CH42	VSS1032
CI42	VSS1033
CJ42	VSS1034
CK42	VSS1035
CL42	VSS1036
CM42	VSS1037
CN42	VSS1038
CO42	VSS1039
CP42	VSS1040
CQ42	VSS1041
CR42	VSS1042
CS42	VSS1043
CT42	VSS1044
CU42	VSS1045
CV42	VSS1046
CW42	VSS1047
CX42	VSS1048
CY42	VSS1049
CA42	VSS1050
CB42	VSS1051
CC42	VSS1052
CD42	VSS1053
CE42	VSS1054
CF42	VSS1055
CG42	VSS1056
CH42	VSS1057
CI42	VSS1058
CJ42	VSS1059
CK42	VSS1060
CL42	VSS1061
CM42	VSS1062
CN42	VSS1063
CO42	VSS1064
CP42	VSS1065
CQ42	VSS1066
CR42	VSS1067
CS42	VSS1068
CT42	VSS1069
CU42	VSS1070
CV42	VSS1071
CW42	VSS1072
CX42	VSS1073
CY42	VSS1074
CA42	VSS1075
CB42	VSS1076
CC42	VSS1077
CD42	VSS1078
CE42	VSS1079
CF42	VSS1080
CG42	VSS1081
CH42	VSS1082
CI42	VSS1083
CJ42	VSS1084
CK42	VSS1085
CL42	VSS1086
CM42	VSS1087
CN42	VSS1088
CO42	VSS1089
CP42	VSS1090
CQ42	VSS1091
CR42	VSS1092
CS42	VSS1093
CT42	VSS1094
CU42	VSS1095
CV42	VSS1096
CW42	VSS1097
CX42	VSS1098
CY42	VSS1099
CA42	VSS1100
CB42	VSS1101
CC42	VSS1102
CD42	VSS1103
CE42	VSS1104
CF42	VSS1105
CG42	VSS1106
CH42	VSS1107
CI42	VSS1108
CJ42	VSS1109
CK42	VSS1110
CL42	VSS1111
CM42	VSS1112
CN42	VSS1113
CO42	VSS1114
CP42	VSS1115
CQ42	VSS1116
CR42	VSS1117
CS42	VSS1118
CT42	VSS1119
CU42	VSS1120
CV42	VSS1121
CW42	VSS1122
CX42	VSS1123
CY42	VSS1124
CA42	VSS1125
CB42	VSS1126
CC42	VSS1127
CD42	VSS1128
CE42	VSS1129
CF42	VSS1130
CG42	VSS1131
CH42	VSS1132
CI42	VSS1133
CJ42	VSS1134
CK42	VSS1135
CL42	VSS1136
CM42	VSS1137
CN42	VSS1138
CO42	VSS1139
CP42	VSS1140
CQ42	VSS1141
CR42	VSS1142
CS42	VSS1143
CT42	VSS1144
CU42	VSS1145
CV42	VSS1146
CW42	VSS1147
CX42	VSS1148
CY42	VSS1149
CA42	VSS1150
CB42	VSS1151
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CF42	VSS1155
CG42	VSS1156
CH42	VSS1157
CI42	VSS1158
CJ42	VSS1159
CK42	VSS1160
CL42	VSS1161
CM42	VSS1162
CN42	VSS1163
CO42	VSS1164
CP42	VSS1165
CQ42	VSS1166
CR42	VSS1167
CS42	VSS1168
CT42	VSS1169
CU42	VSS1170
CV42	VSS1171
CW42	VSS1172
CX42	VSS1173
CY42	VSS1174
CA42	VSS1175
CB42	VSS1176
CC42	VSS1177
CD42	VSS1178
CE42	VSS1179
CF42	VSS1180
CG42	VSS1181
CH42	VSS1182
CI42	VSS1183
CJ42	VSS1184
CK42	VSS1185
CL42	VSS1186
CM42	VSS1187
CN42	VSS1188
CO42	VSS1189
CP42	VSS1190
CQ42	VSS1191
CR42	VSS1192
CS42	VSS1193
CT42	VSS1194
CU42	VSS1195
CV42	VSS1196
CW42	VSS1197
CX42	VSS1198
CY42	VSS1199
CA42	VSS1200
CB42	VSS1201
CC42	VSS1202
CD42	VSS1203
CE42	VSS1204
CF42	VSS1205
CG42	VSS1206
CH42	VSS1207
CI42	VSS1208
CJ42	VSS1209
CK42	VSS1210
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CM42	VSS1212
CN42	VSS1213
CO42	VSS1214
CP42	VSS1215
CQ42	VSS1216
CR42	VSS1217
CS42	VSS1218
CT42	VSS1219
CU42	VSS1220
CV42	VSS1221
CW42	VSS1222
CX42	VSS1223
CY42	VSS1224
CA42	VSS1225
CB42	VSS1226
CC42	VSS1227
CD42	VSS1228
CE42	VSS1229
CF42	VSS1230
CG42	VSS1231
CH42	VSS1232
CI42	VSS1233
CJ42	VSS1234
CK42	VSS1235
CL42	VSS1236
CM42	VSS1237
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CO42	VSS1239
CP42	VSS1240
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CR42	VSS1242
CS42	VSS1243
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CV42	VSS1246
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CX42	VSS1248
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CA42	VSS1250
CB42	VSS1251
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CF42	VSS1255
CG42	VSS1256
CH42	VSS1257
CI42	VSS1258
CJ42	VSS1259
CK42	VSS1260
CL42	VSS1261
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CO42	VSS1264
CP42	VSS1265
CQ42	VSS1266
CR42	VSS1267
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CF42	VSS1280
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CS42	VSS1293
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CU42	VSS1295
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CN42	VSS1313
CO42	VSS1314
CP42	VSS1315
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CR42	VSS1317
CS42	VSS1318
CT42	VSS1319
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CF42	VSS1505
CG42	VSS1506
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CK42	VSS1510
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CN42	VSS1513
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CP42	VSS1515
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CR42	VSS1517
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CT42	VSS1519
CU42	VSS1520
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CY42	VSS1524
CA42	VSS1525
CB42	VSS1526
CC42	VSS1527
CD42	VSS1528
CE42	VSS1529
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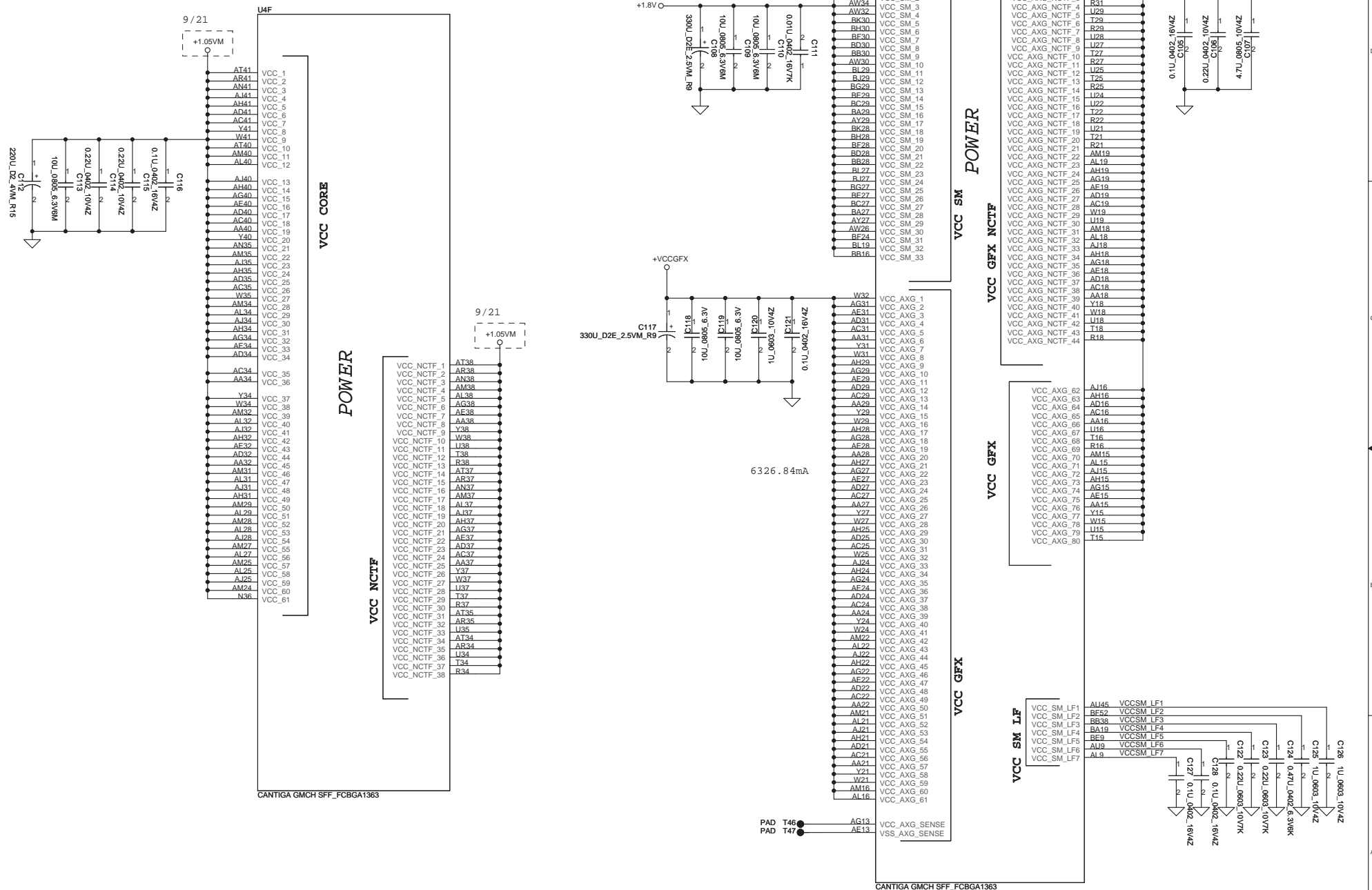
Strap Pin Table	
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chipser suite with no confidentiality 1 =(TLS)chipser suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



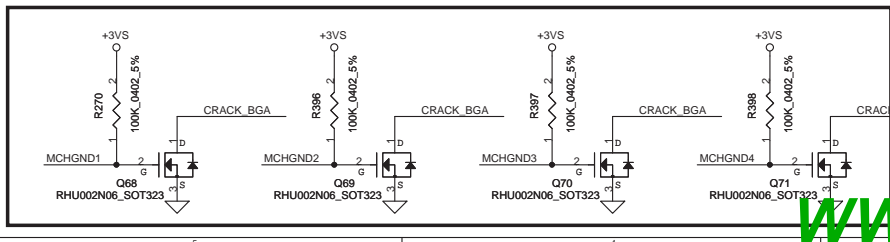
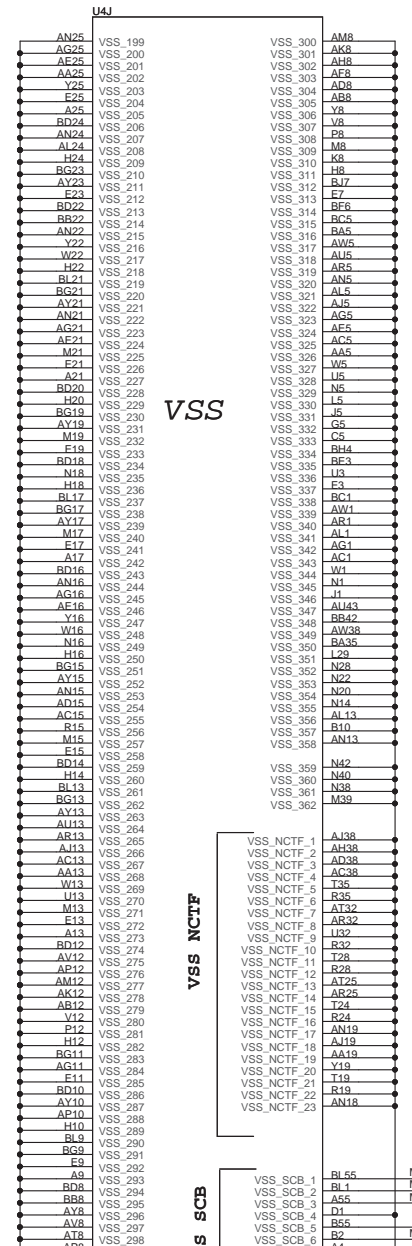
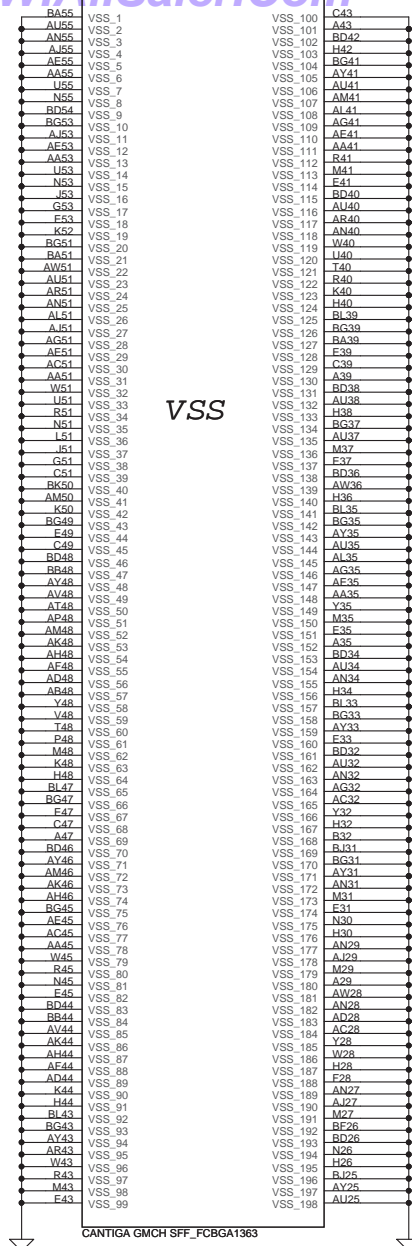


WWW.AISaerCo!

Extlnal Graphic: 1210.34mA
integrated Graphic: 1930.4mA



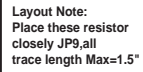
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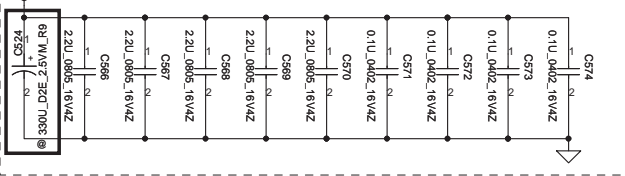
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Change C131 to 330uF. 9/26

The schematic diagram illustrates a 10-bit DAC circuit. It features a resistor ladder network with 10 bits of resolution. The ladder is connected to a +0.9V supply. The output of the ladder is connected to a buffer op-amp, which is configured with a feedback resistor of 10kΩ and an input resistor of 10kΩ. The output of the buffer is connected to a 10kΩ load resistor. The circuit is powered by a +0.9V supply and a -0.9V supply.



WWW.AllSaler.Com

+1.8V
Ω Reserve C524. 9/26

(+0.9V)

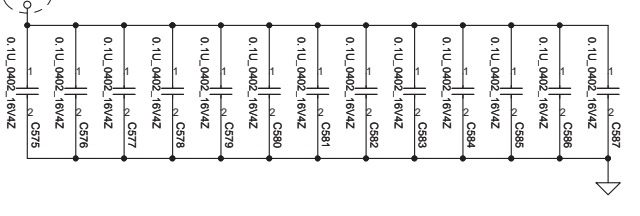
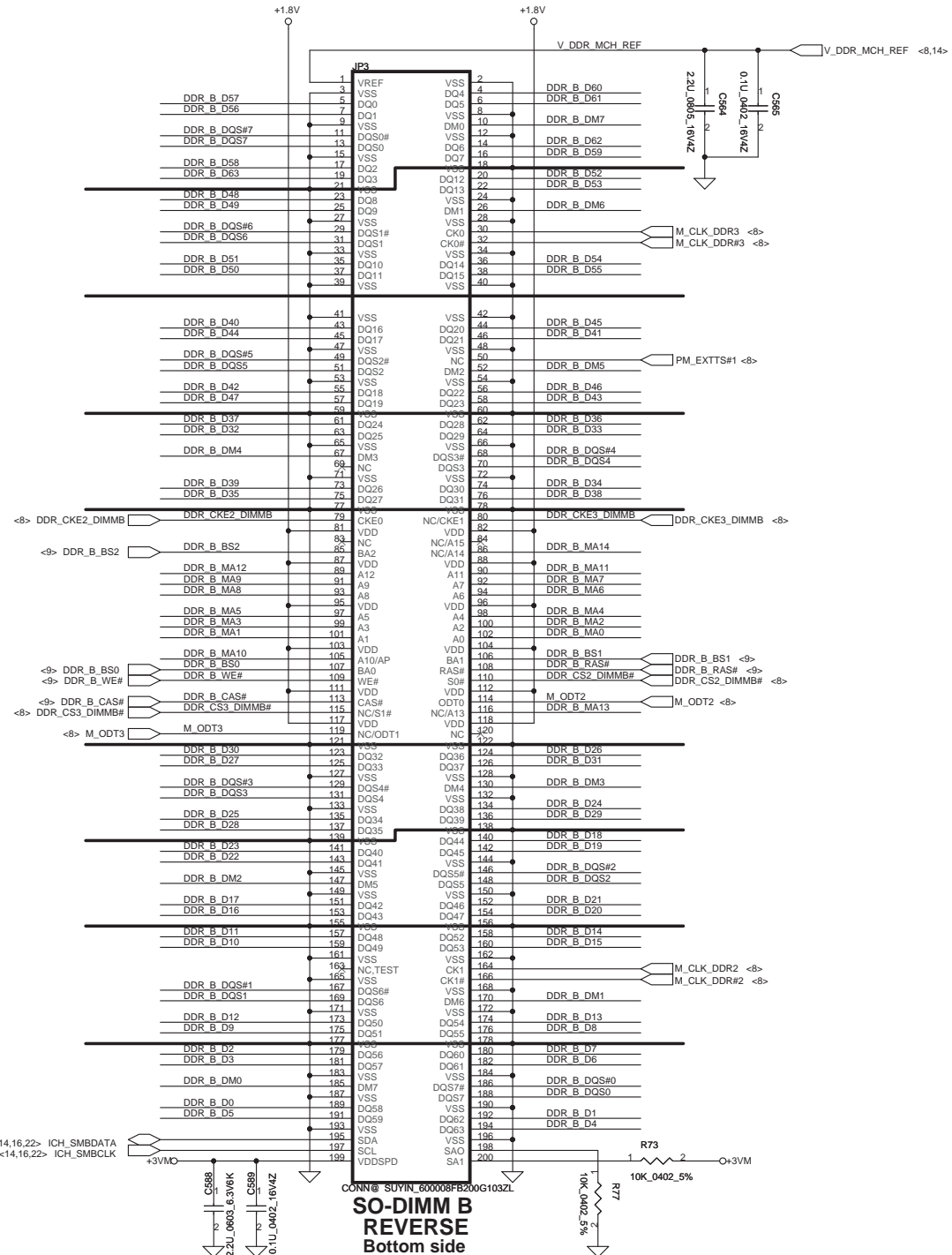


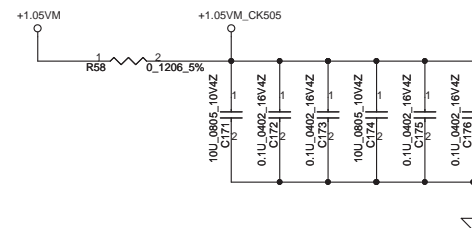
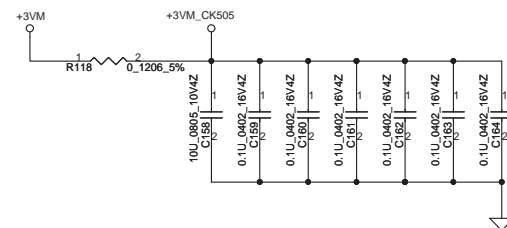
Figure 10-10 shows the DDR B and DDR C DIMM connections to the R80. The DDR B and DDR C DIMM connections are shown in the table below.

DDR B MA1	1	4	4	1	DDR B MA9
DDR B MA3	2	3	3	2	DDR B MA12
56_0404_4P2R_5%		RP22	RP23		56_0404_4P2R_5%
DDR B BS0	1	4	4	1	DDR CKE3 DIMMB
DDR B MA10	2	3	3	2	DDR B MA14
56_0404_4P2R_5%		RP24	RP25		56_0404_4P2R_5%
DDR B MA0	1	4	4	1	DDR B MA5
DDR B BS1	2	3	3	2	DDR B MA8
56_0404_4P2R_5%		RP26	RP27		56_0404_4P2R_5%
DDR B RAS#	1	4	4	1	DDR B MA7
DDR CS2 DIMMB#	2	3	3	2	DDR B MA6
56_0404_4P2R_5%		RP28	RP29		56_0404_4P2R_5%
DDR B CAS#	1	4	4	1	DDR B MA4
DDR B WE#	2	3	3	2	DDR B MA2
56_0404_4P2R_5%		RP30	RP31		56_0404_4P2R_5%
DDR CS3 DIMMB#	1	4	4	1	M ODT2
M ODT3	2	3	3	2	DDR B MA13
56_0404_4P2R_5%		RP32	RP33		56_0404_4P2R_5%
DDR B MA11	1	4	4	1	DDR B BS2
56_0402_5%		R80	RP34		DDR CKE2 DIMMB



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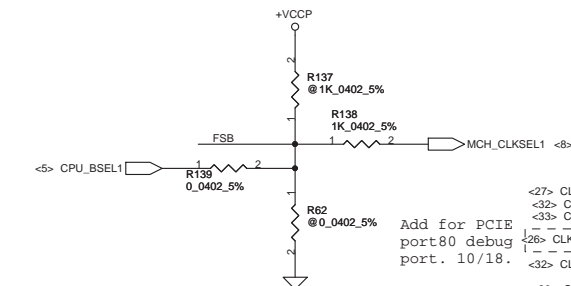
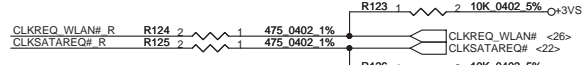
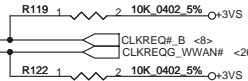
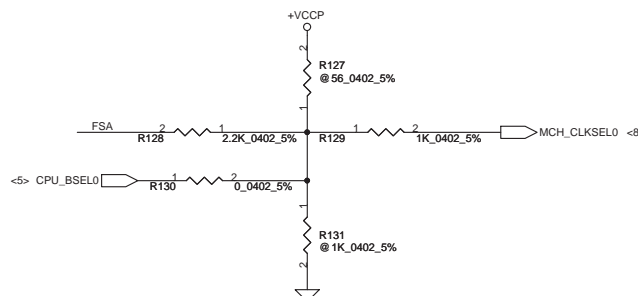
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	FSB MHz	SRC MHz	PCI MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3



C156	2	1 CLK 48M ICH @ 5P_0402_50V8C
C157	1	2 CLK 14M ICH 12P_0402_50V8J
C165	2	1 CLK PCI ICH @ 4.7P_0402_50V8C
C166	1	2 CLK 14M XBG 12P_0402_50V8J
C167	2	1 CLK PCI EC @ 4.7P_0402_50V8C
C168	2	1 CLK PCI TCG @ 4.7P_0402_50V8C
C169	2	1 CLK PCI 1394 @ 5P_0402_50V8C
C170	2	1 CLK PCI DMI @ 5P_0402_50V8C

Mount C157 & C166 tp solve
LWANT noise issue 1/22

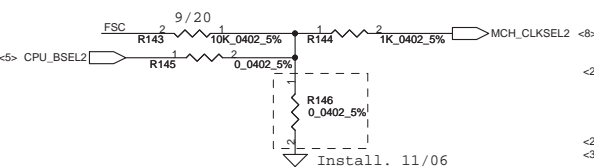
Place close to U5



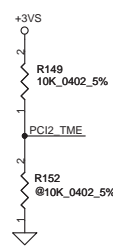
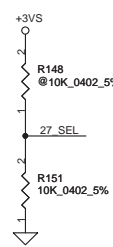
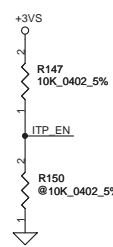
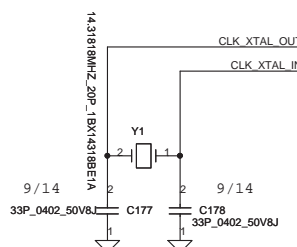
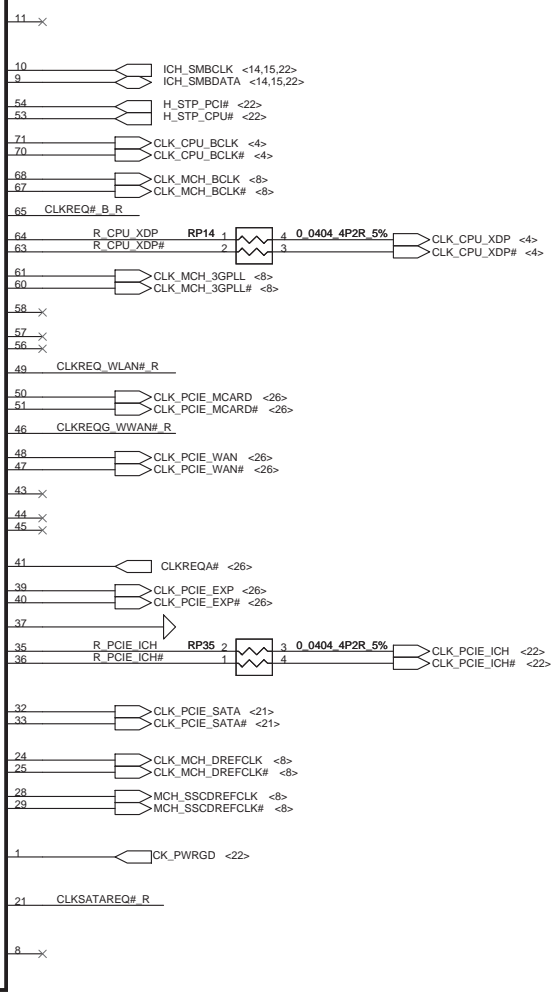
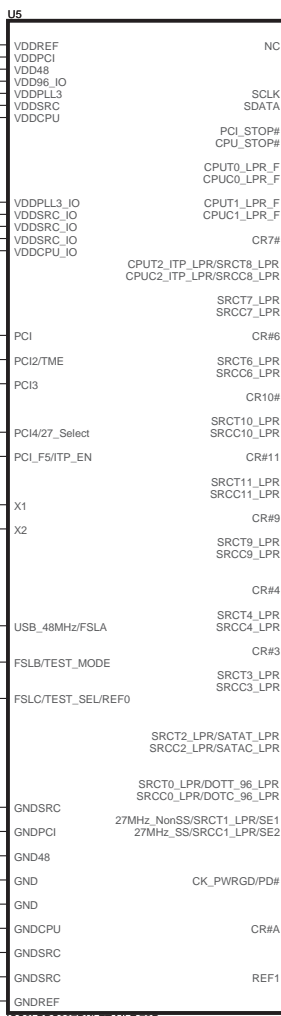
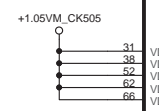
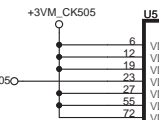
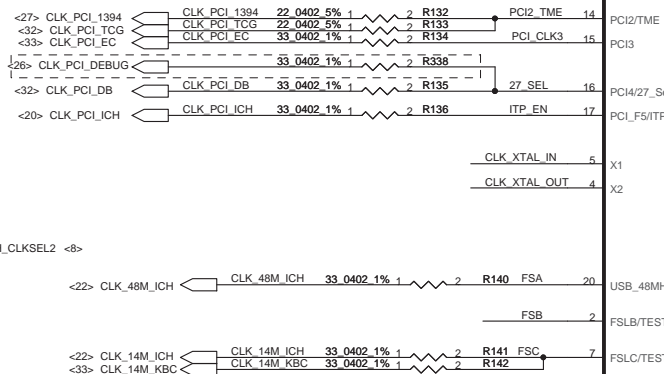
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Add for PCIE
port80 debug <26> CLK
port. 10/18. <32> CLK

```



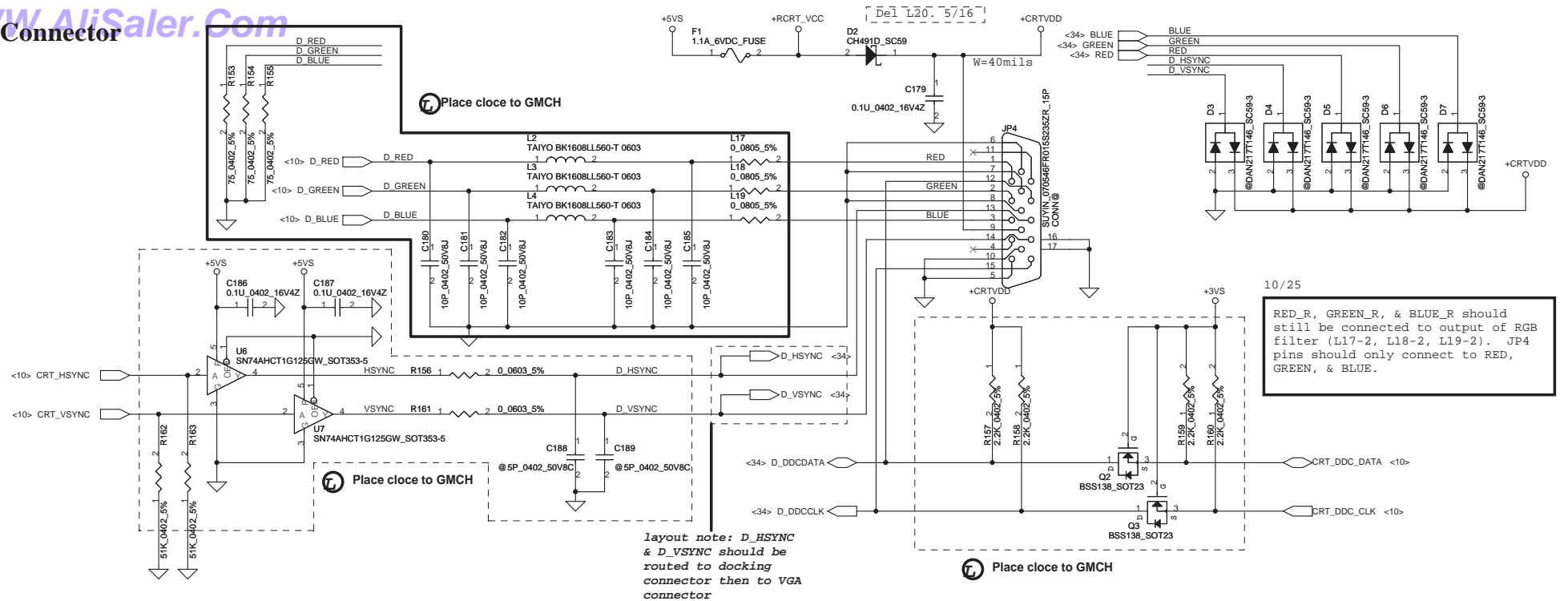
➤ Install. 11/06



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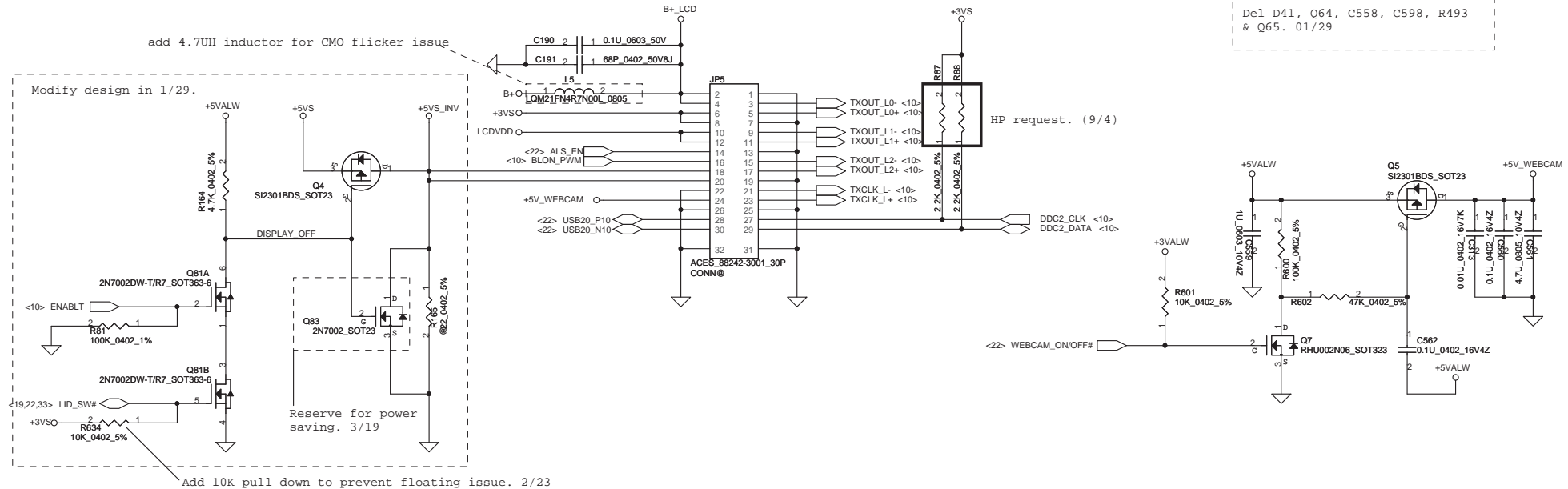
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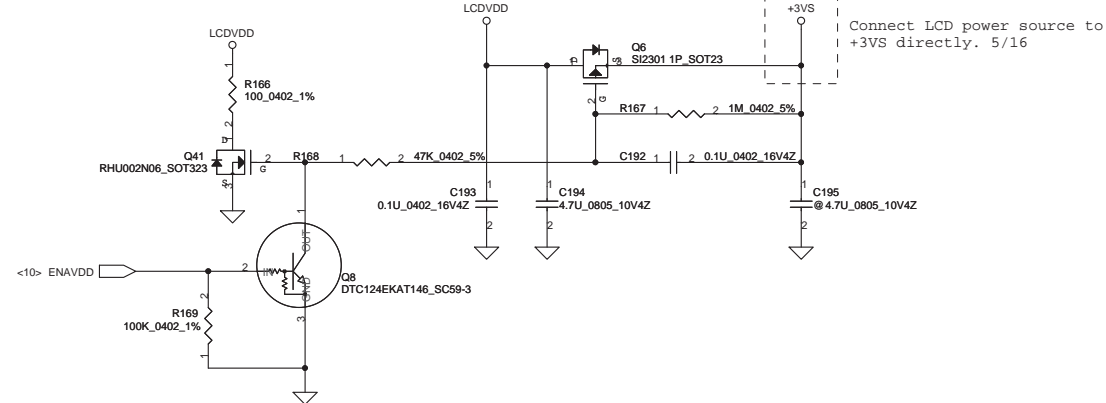


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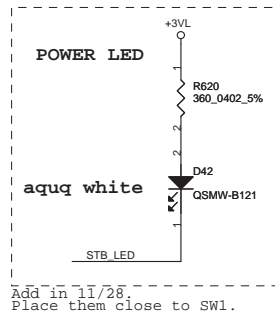
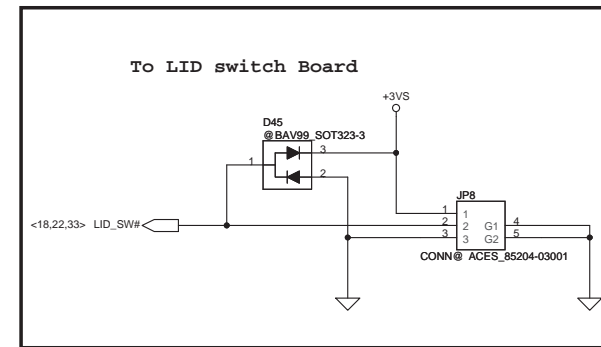
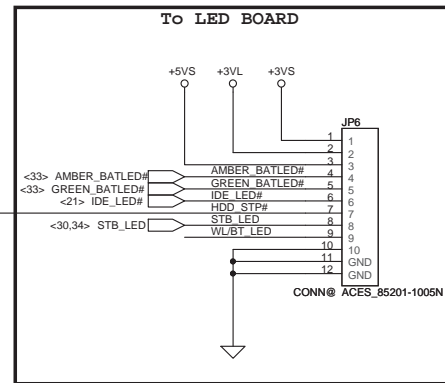
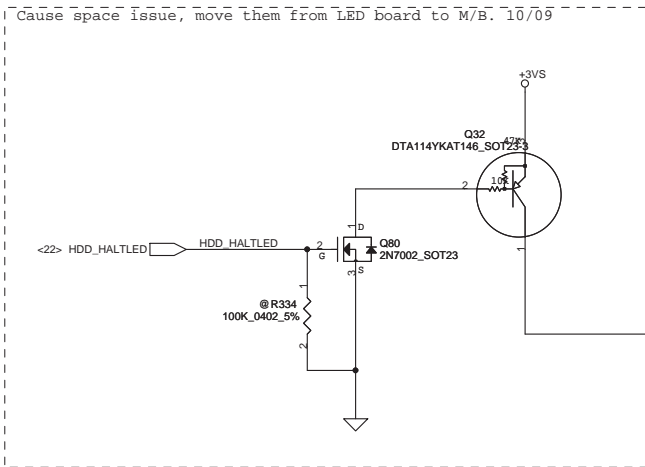
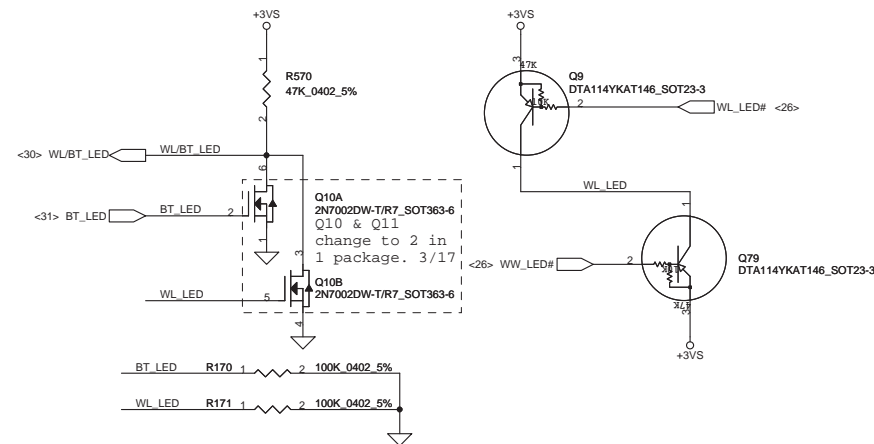
LCD/PANEL BD. CONN.



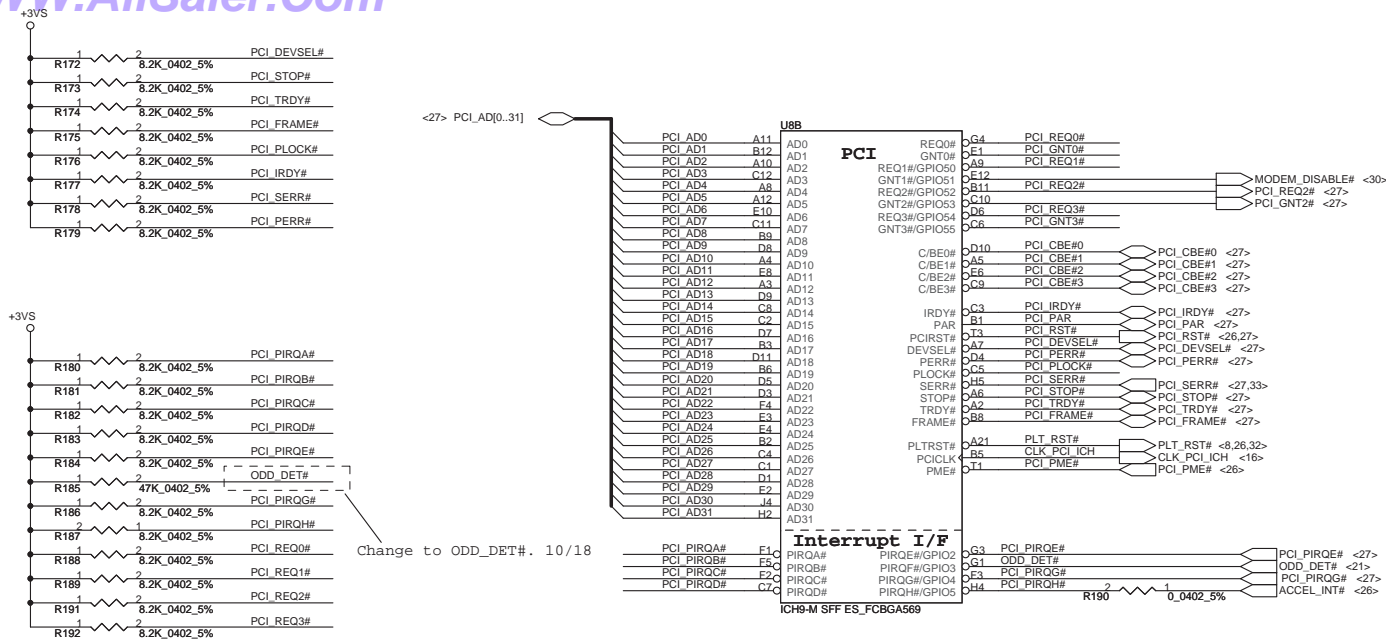
LCD POWER CIRCUIT



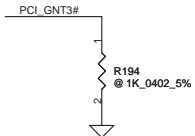
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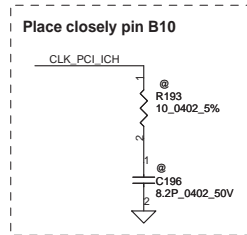
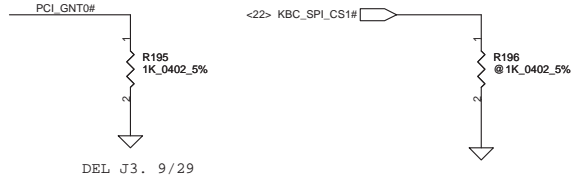
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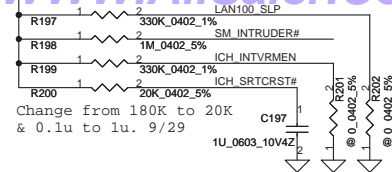


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



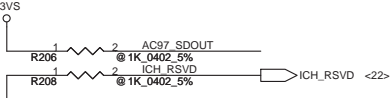
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC



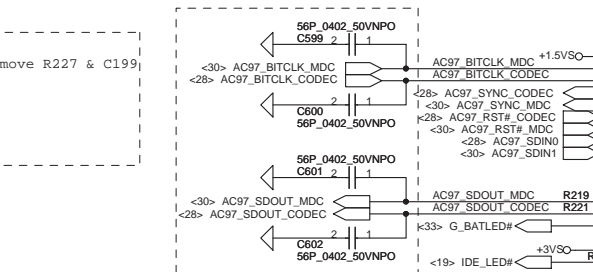


ICH_RSVD	HDA_SDOUT_CODEC	Description
0	0	RV
0	1	XOR
1	0	Normal (D
1	1	PCIE Bit

XOR CHAIN ENTRANCE STRAP:RSVD

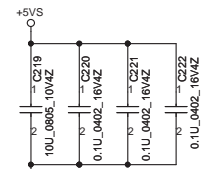
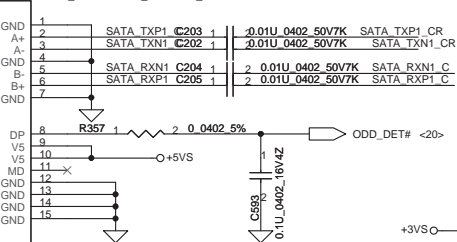


Add C599 ~ C602 to solve WWAN noise issue. 1/23



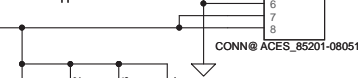
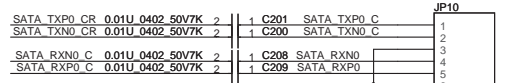
SATA CD-ROM Connector

JP9
CONN@ OCTEK_SAT-22DE1G_NRSUYIN_127059FR022S305ZL

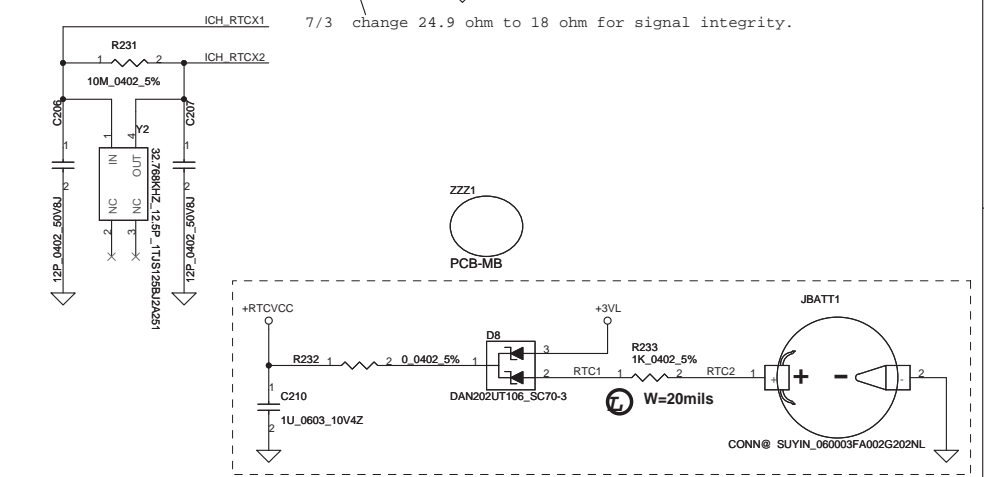
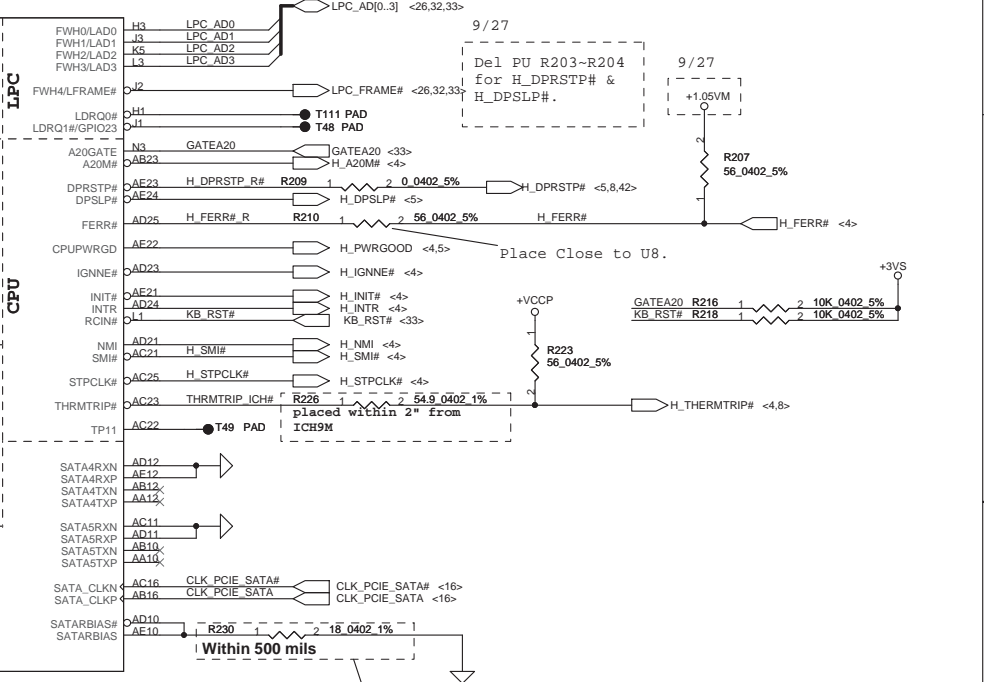
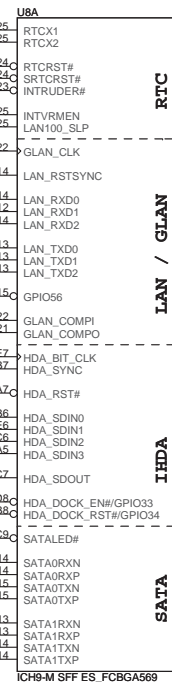


Place component's
closely SATA
CONN. (JP9)

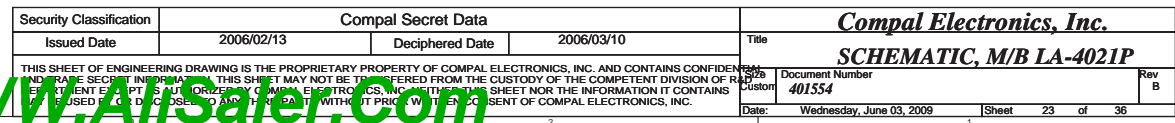
1.8" SATA HDD CONN

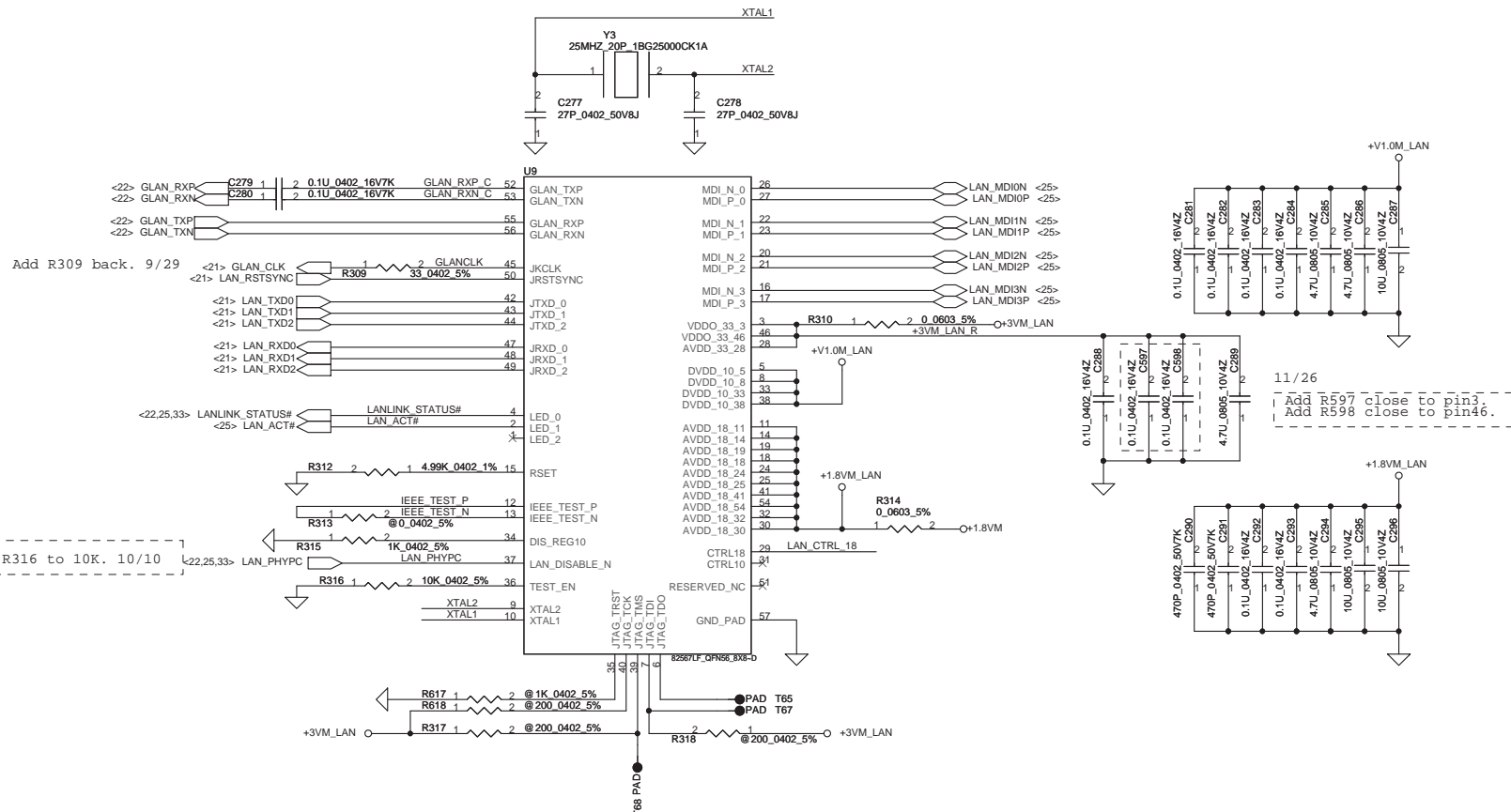
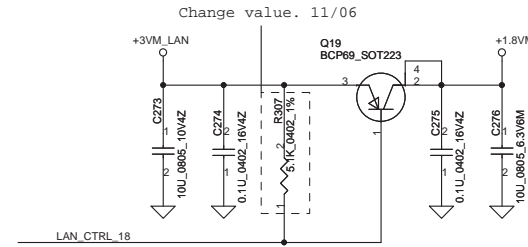
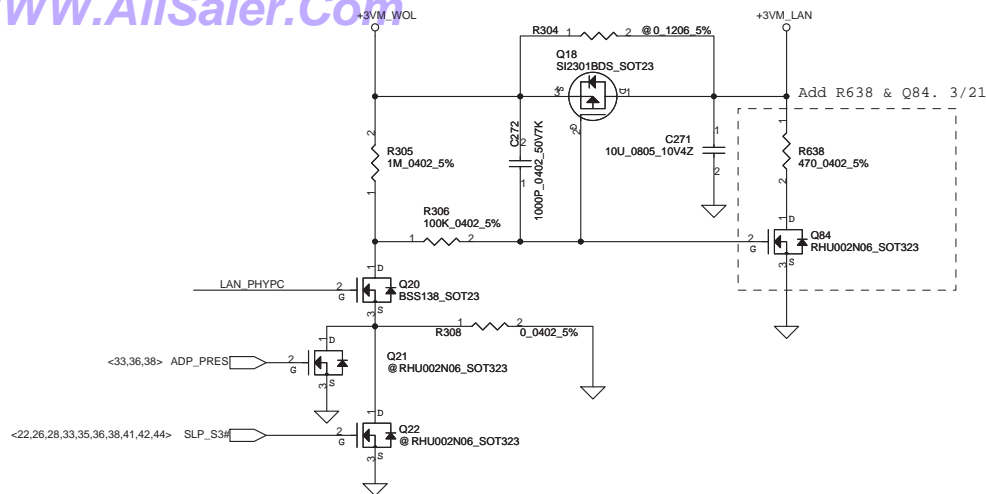


Place component's
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CONN. (JP10)

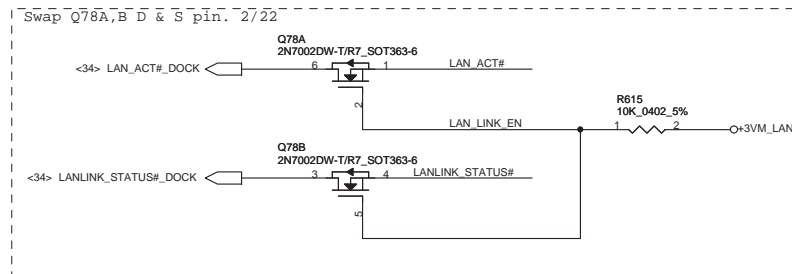


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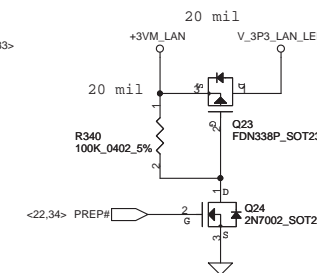
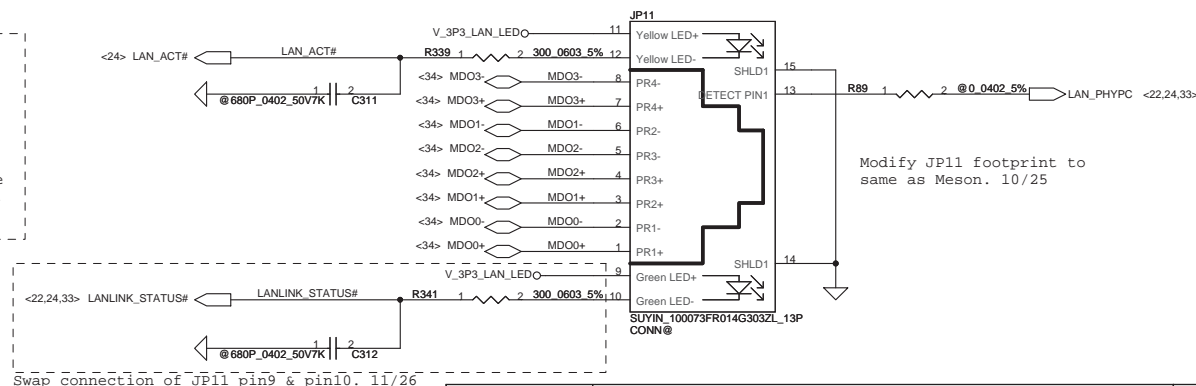
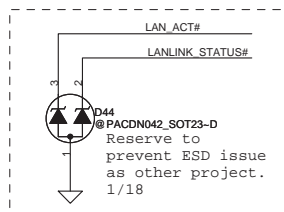
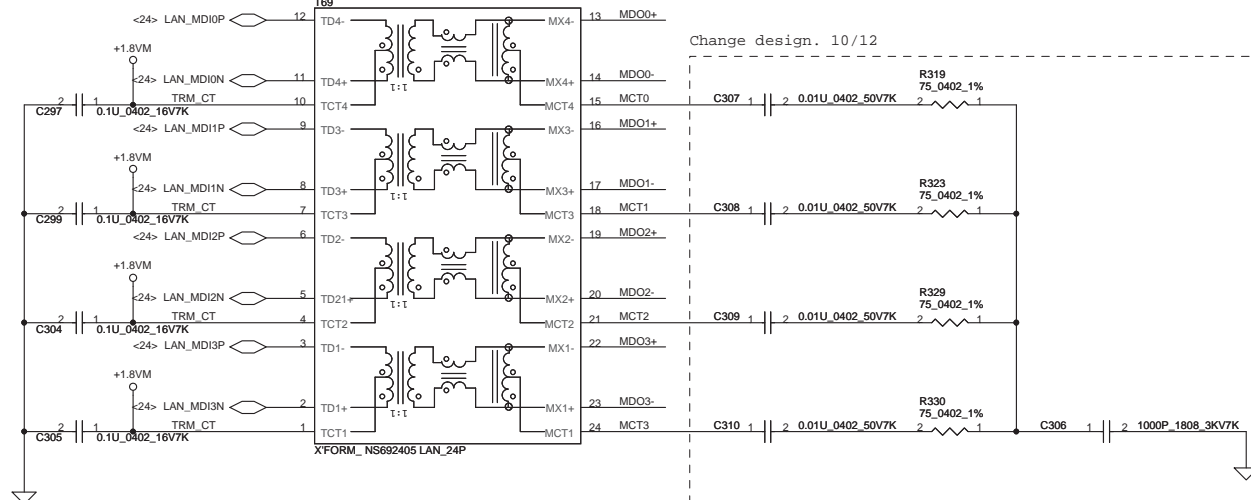


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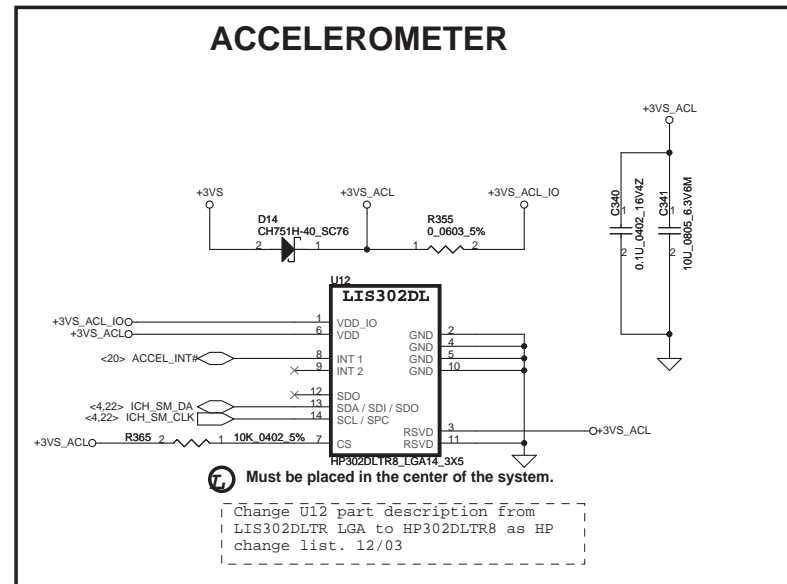
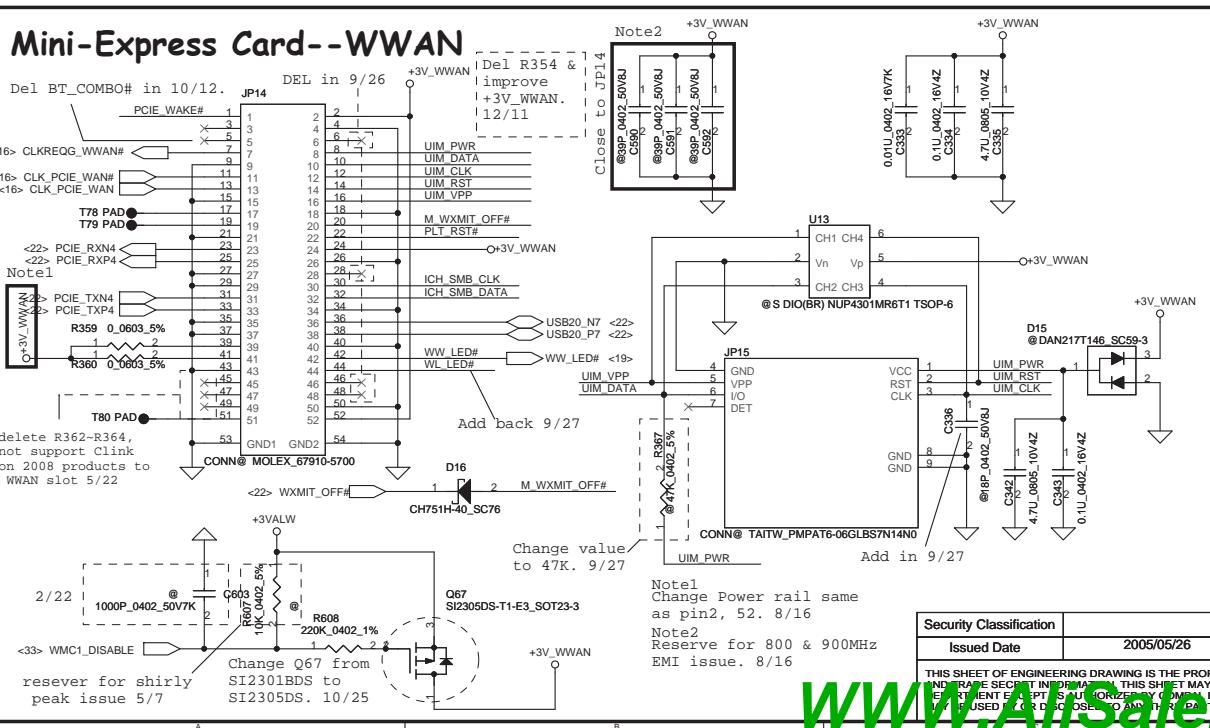
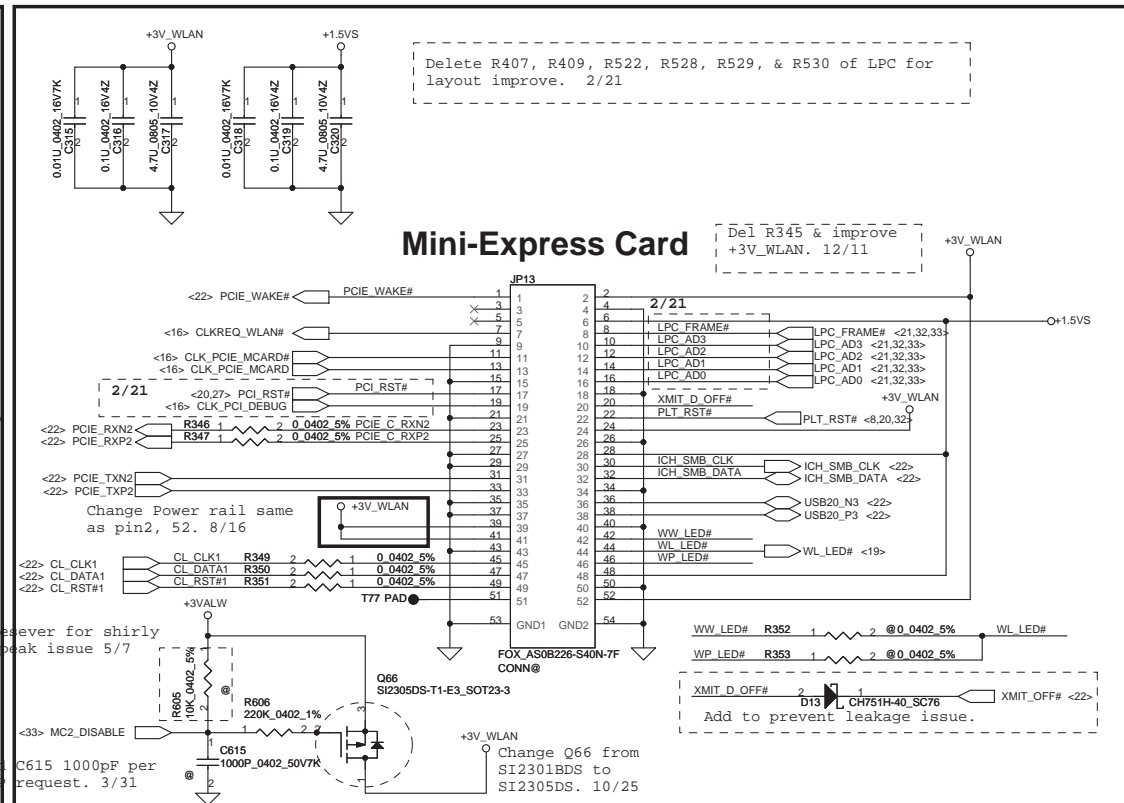
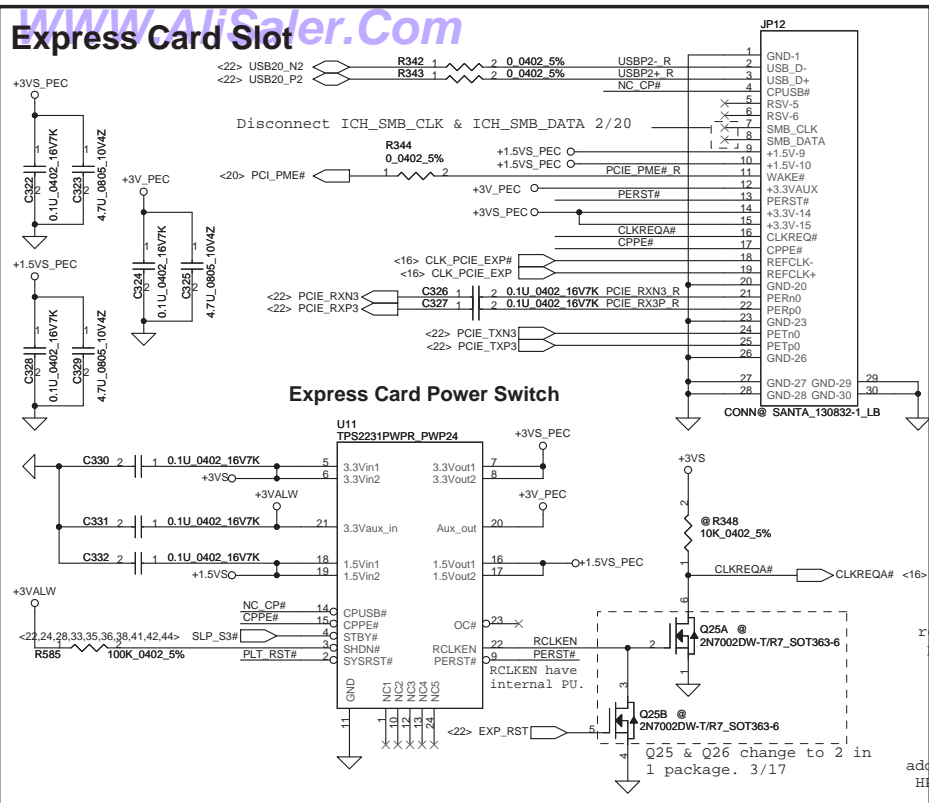
Delete all termination cause they are already inside BOAZMAN. 9/28

Pin Swap. 10/05
Swap P & N. 10/09

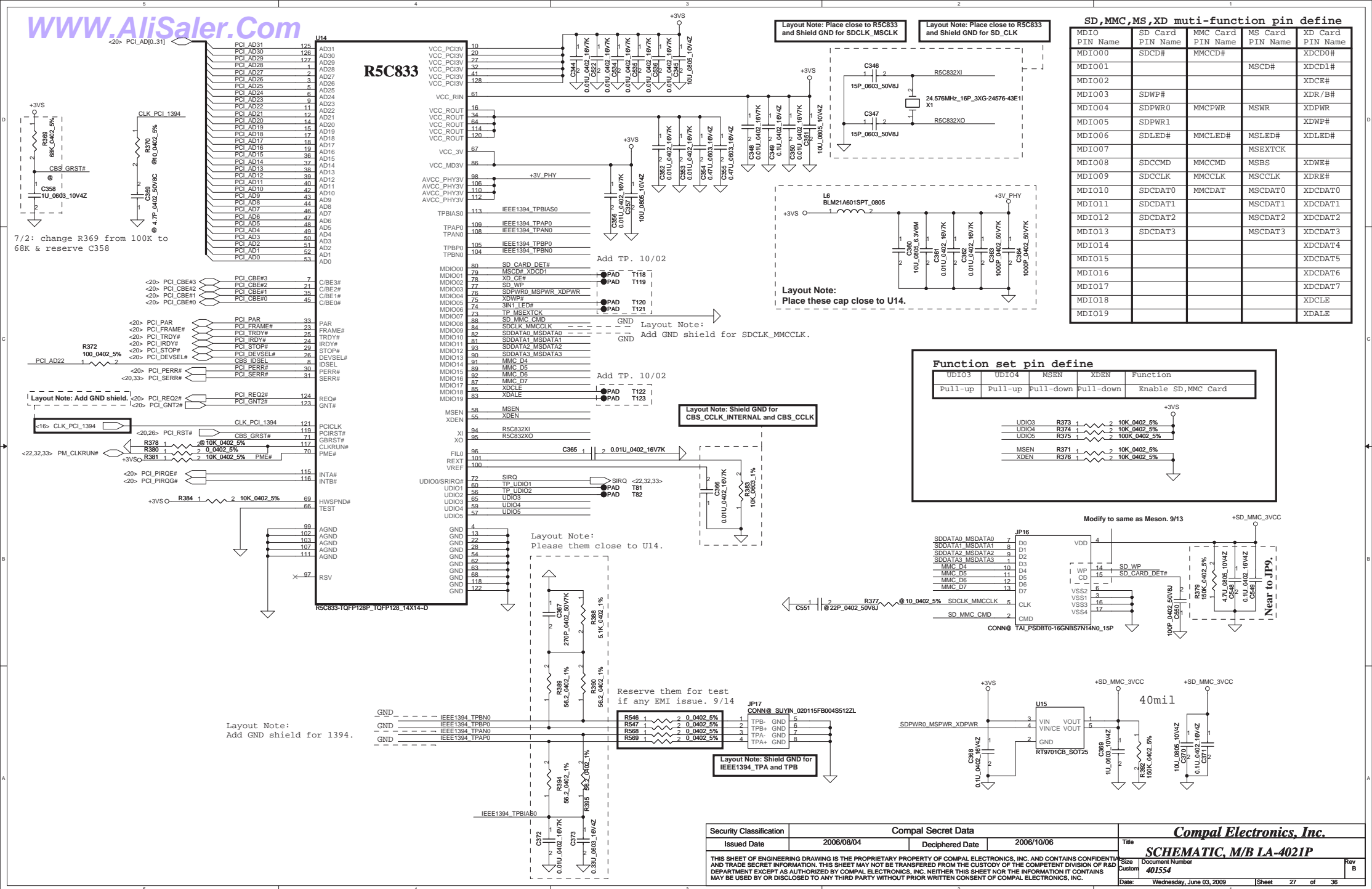


Swap connection of JP11 pin9 & pin10. 11/26

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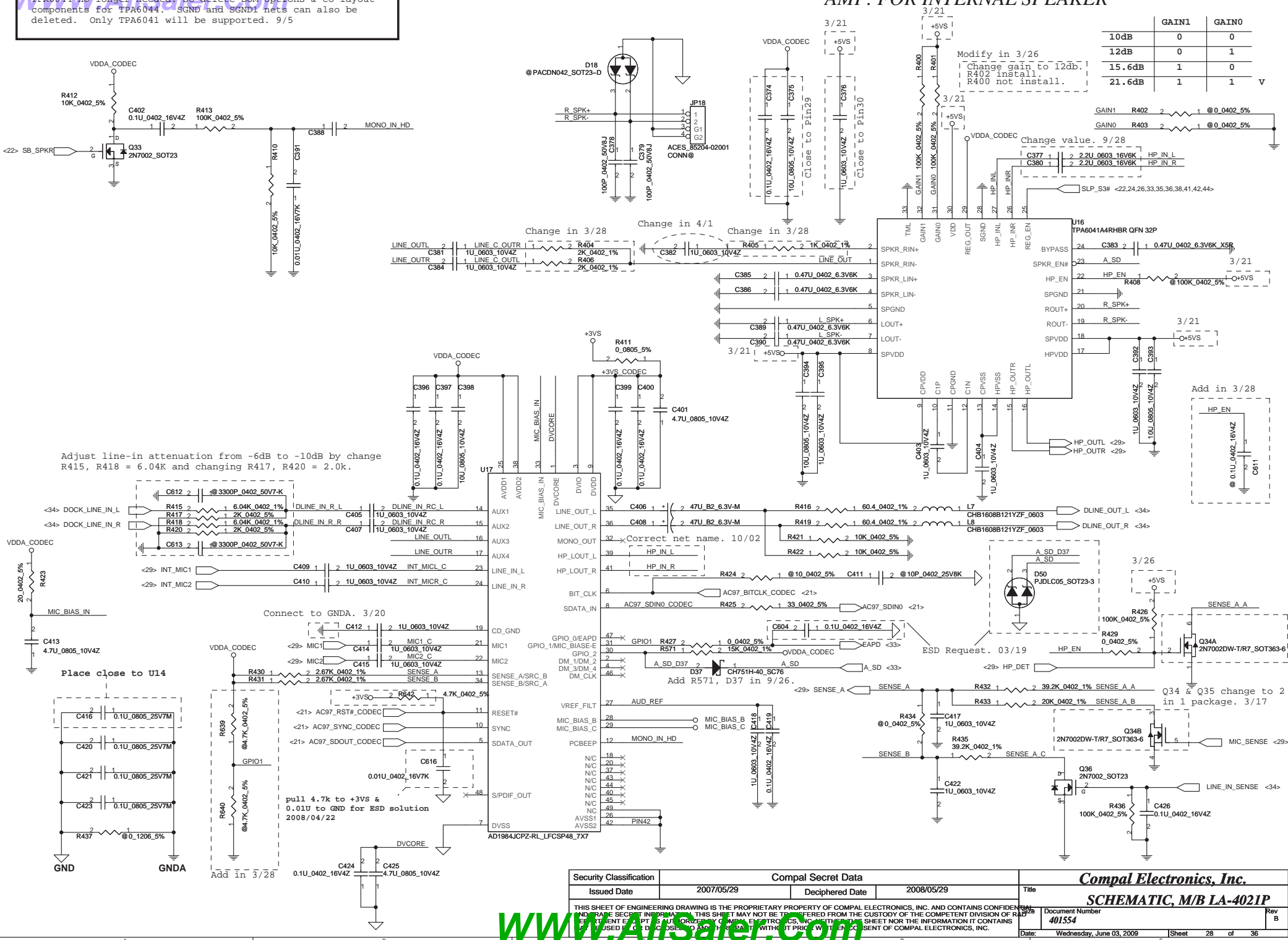


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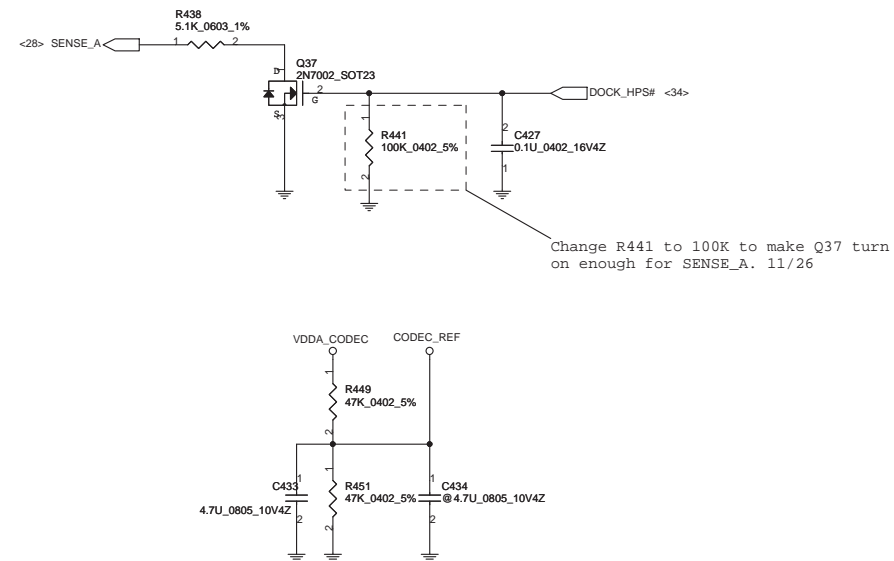
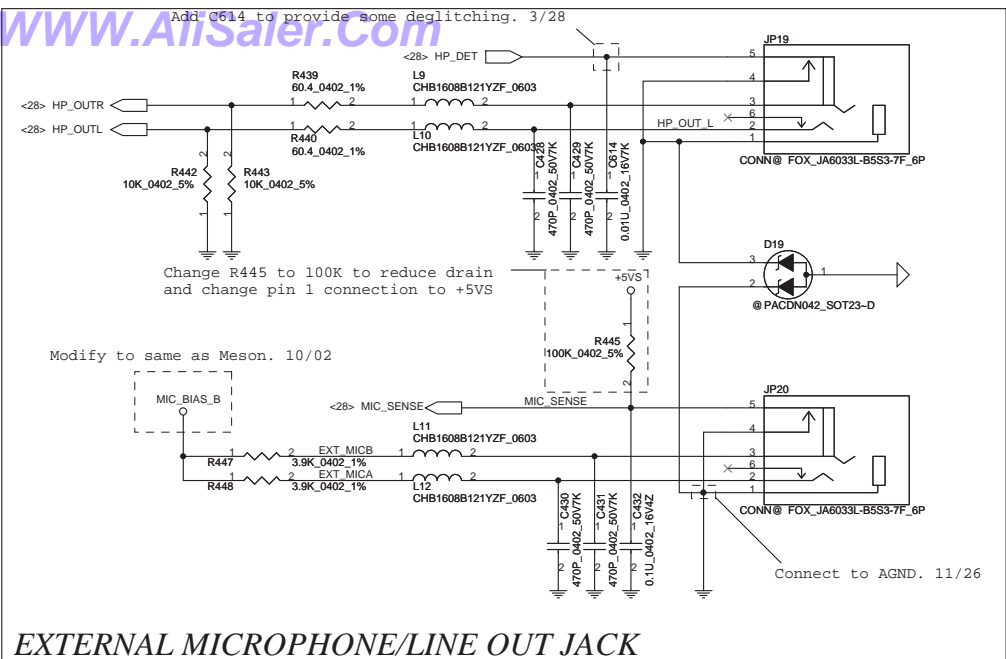


TPA6044 no longer needed. So delete BOM options & co-layout components for TPA6044. SGND and SGND1 nets can also be deleted. Only TPA6041 will be supported. 9/5

AMP. FOR INTERNAL SPEAKER

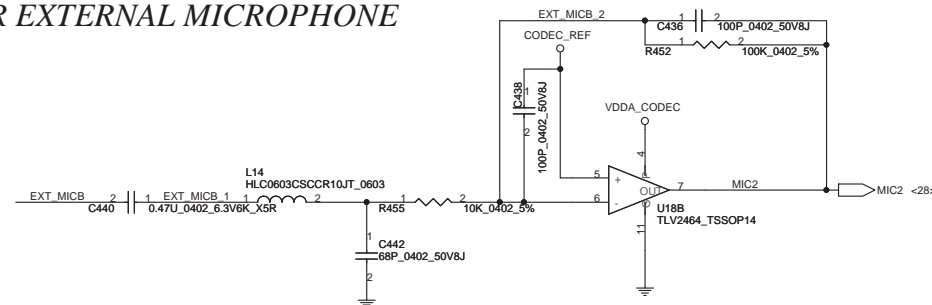
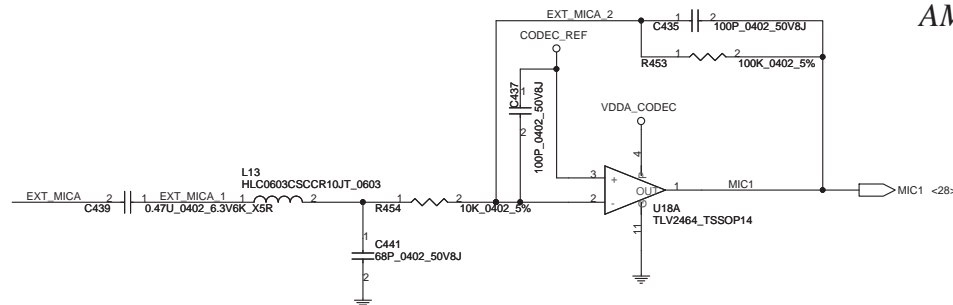


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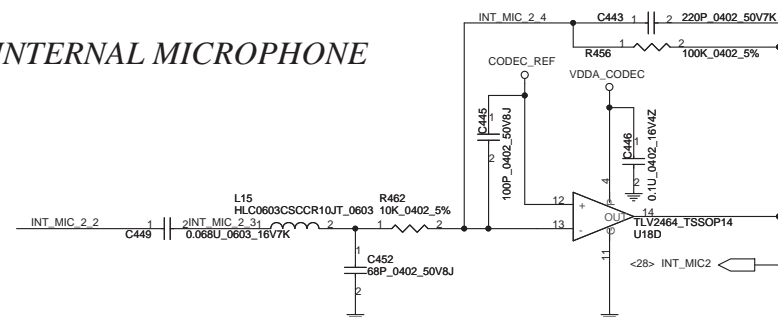
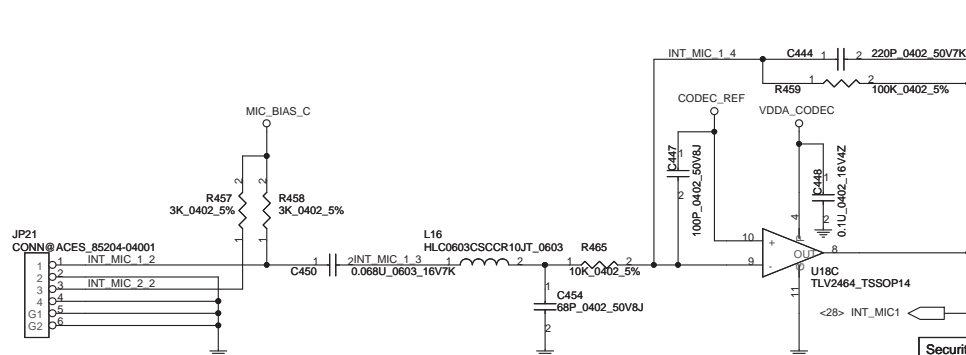


EXTERNAL MICROPHONE/LINE OUT JACK

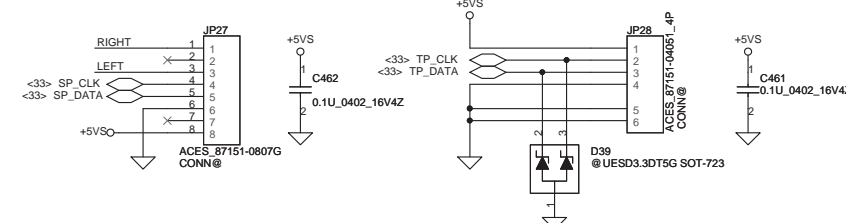
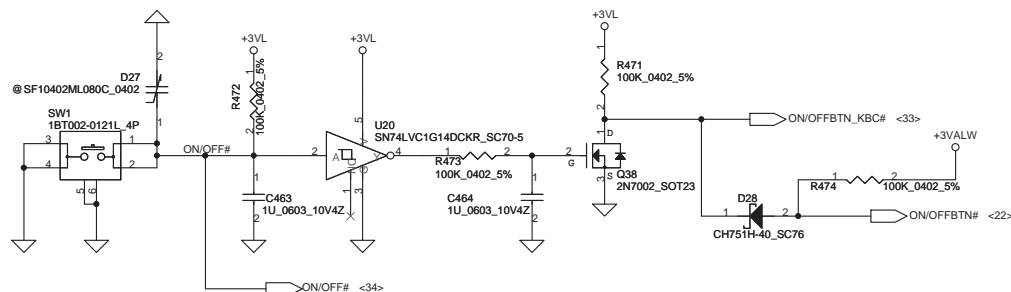
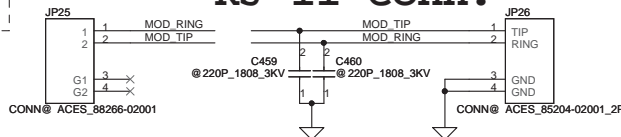
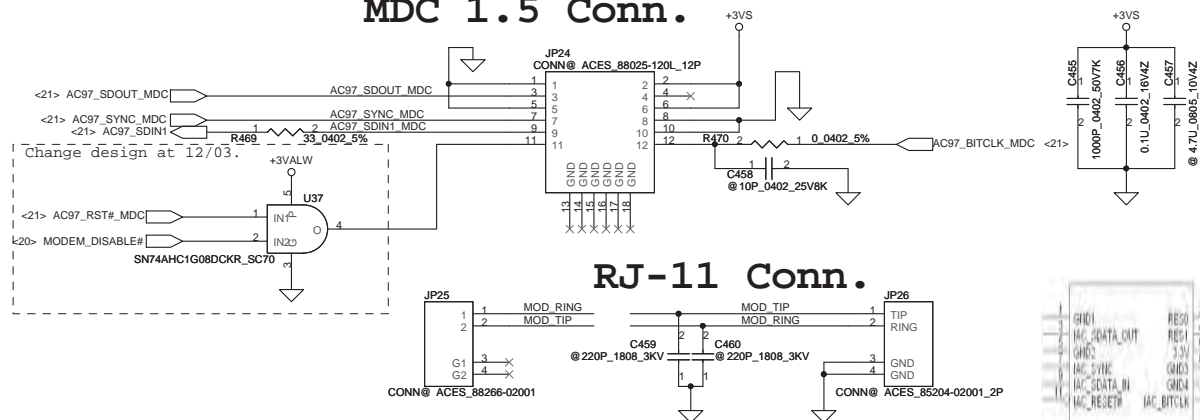
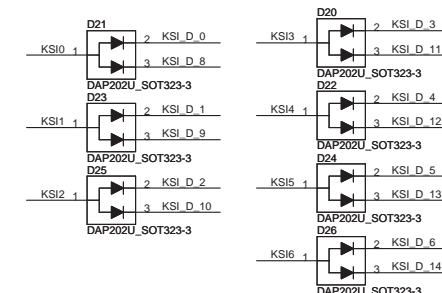
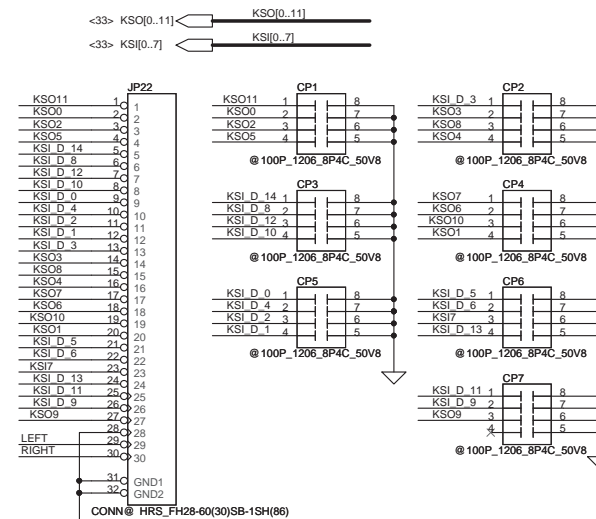
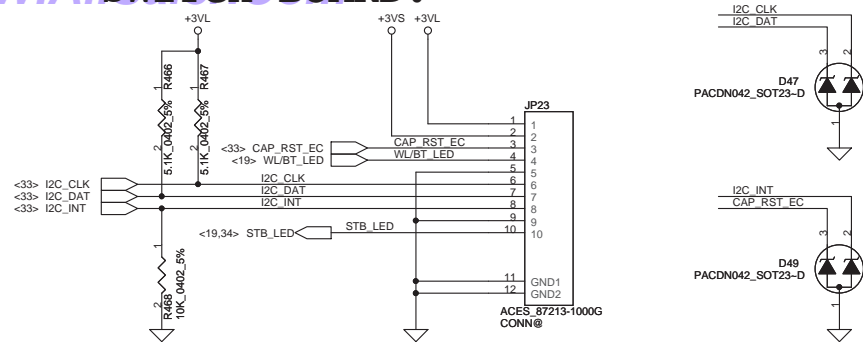
AMP. FOR EXTERNAL MICROPHONE



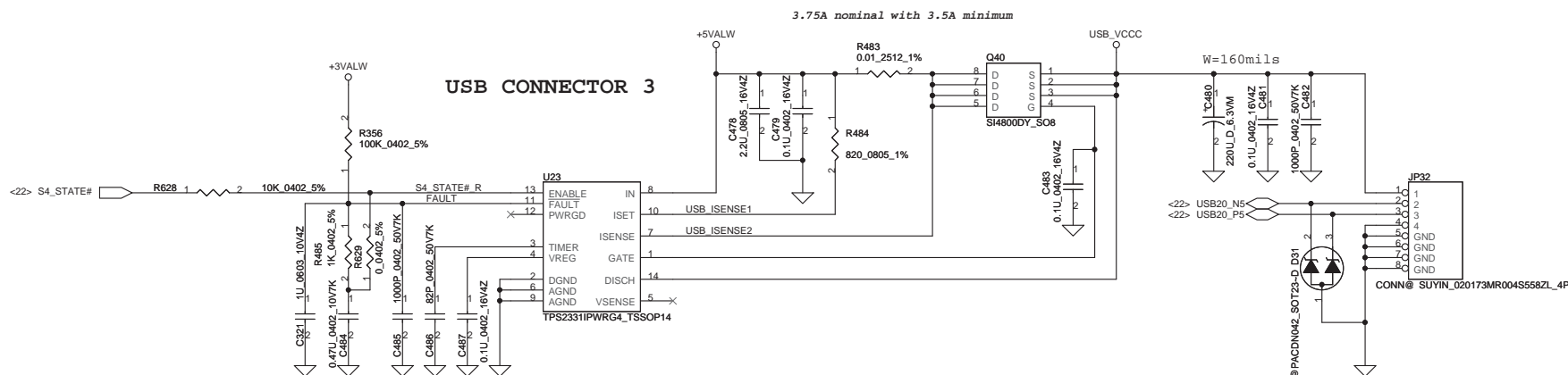
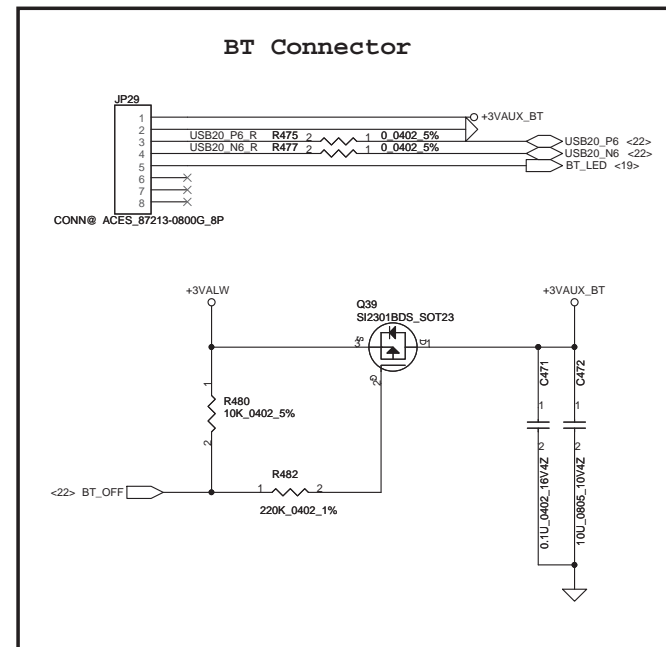
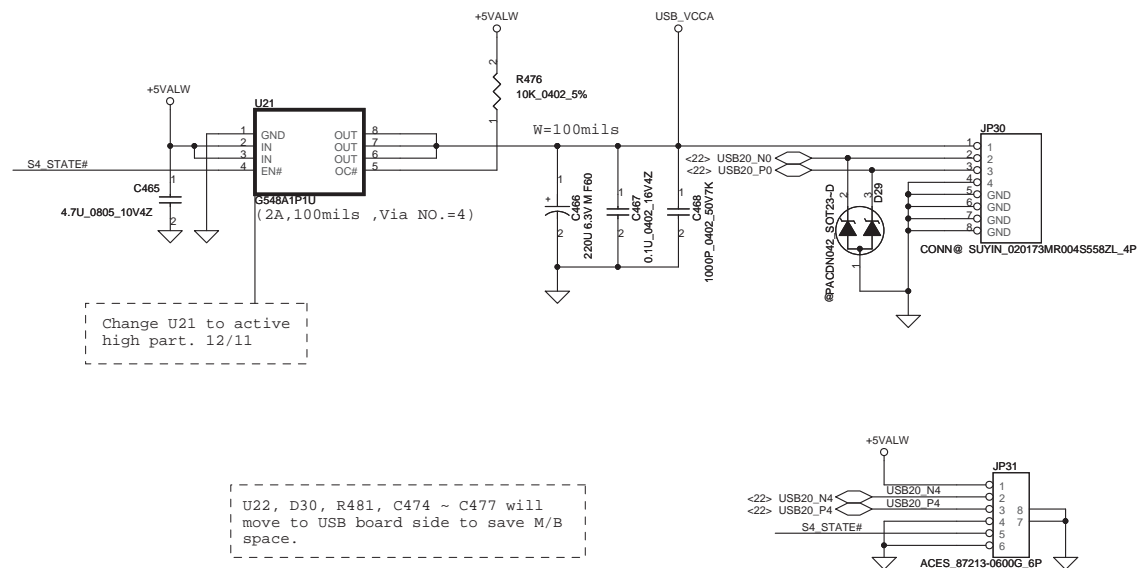
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Change for S11 to prevent USB power short to GND cause system shutdown. 0130

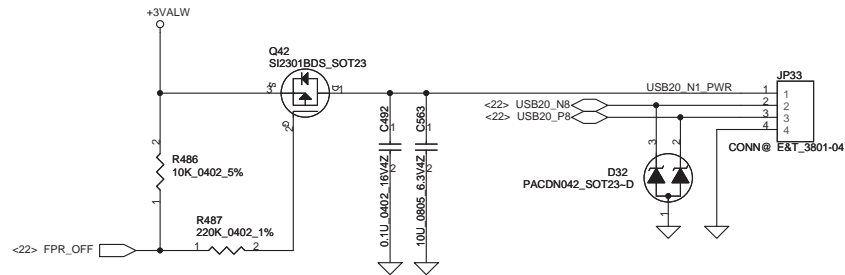
Change C486 from 2200pF to 680pF.
Change C321 from 1000pF to 1uF.
Change R356 from 10K to 100K.
Change C484 from 1000pF to 0.47uF.
Change R484 from 1K to 820.

Currently power USB will not enable after OCP, so add R629 make it enable after OCP free.

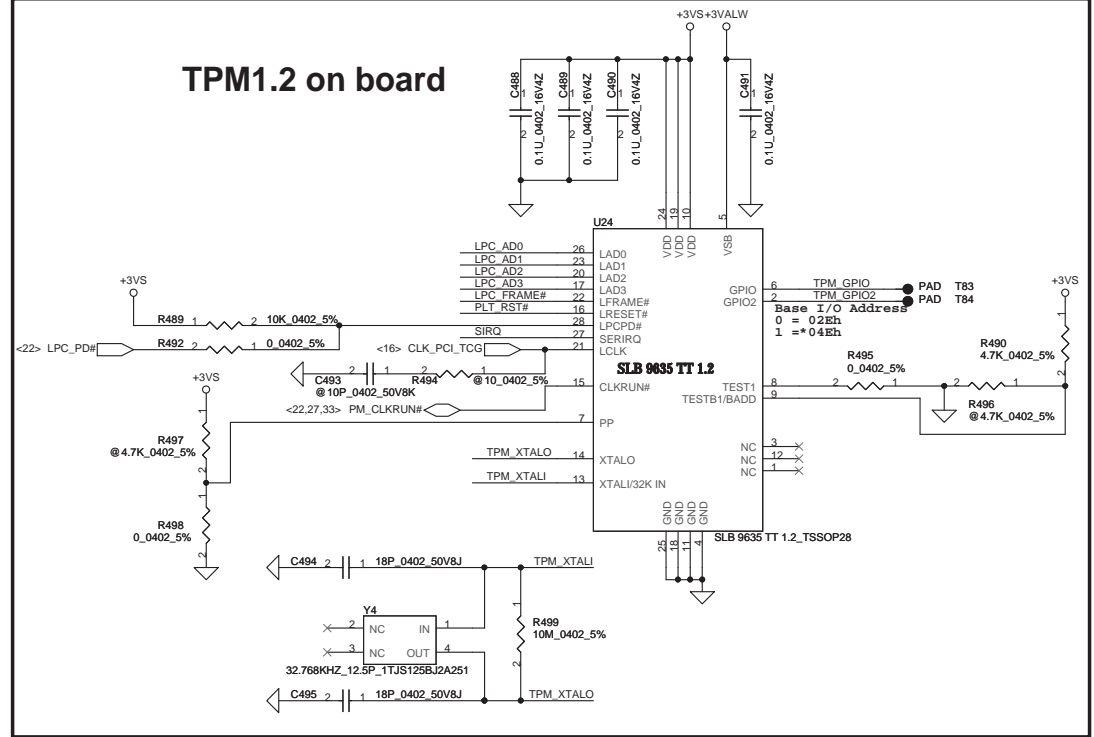
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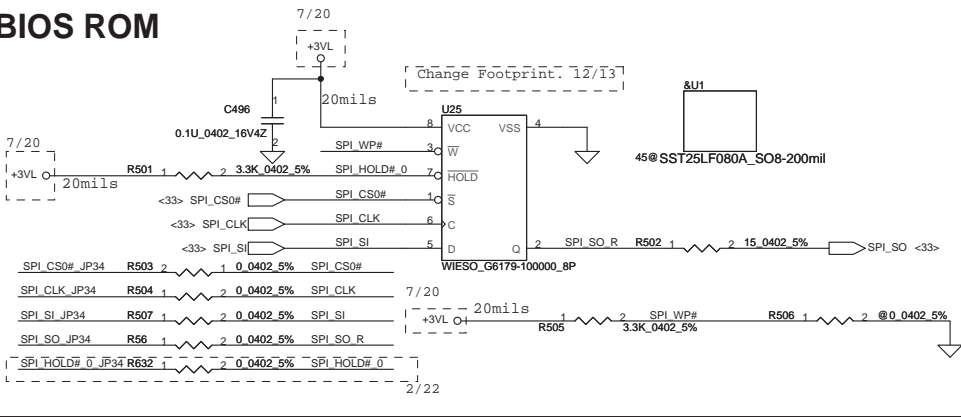
Finger printer



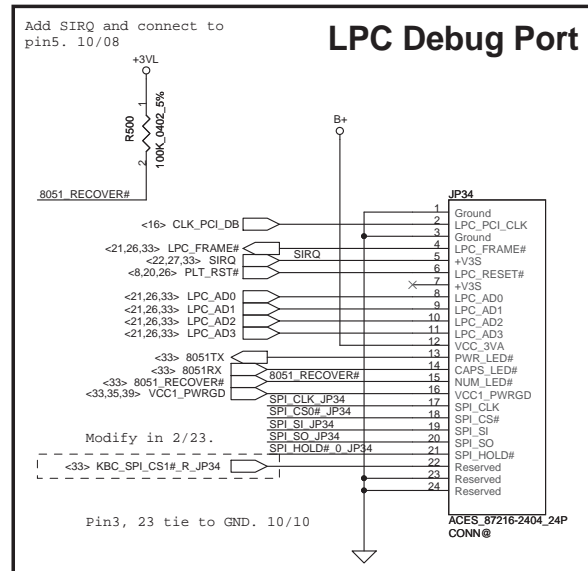
TPM1.2 on board



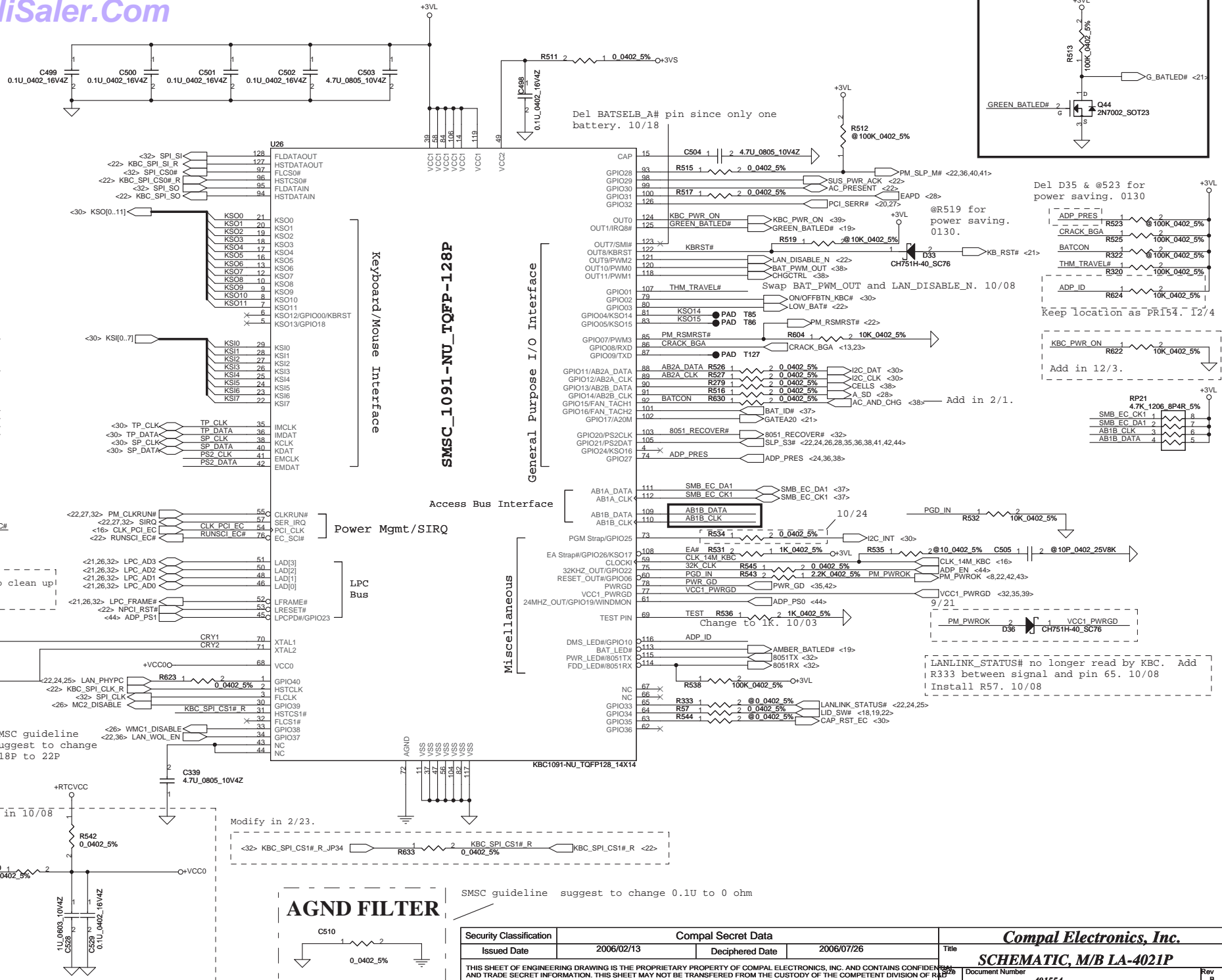
BIOS ROM

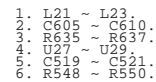


LPC Debug Port

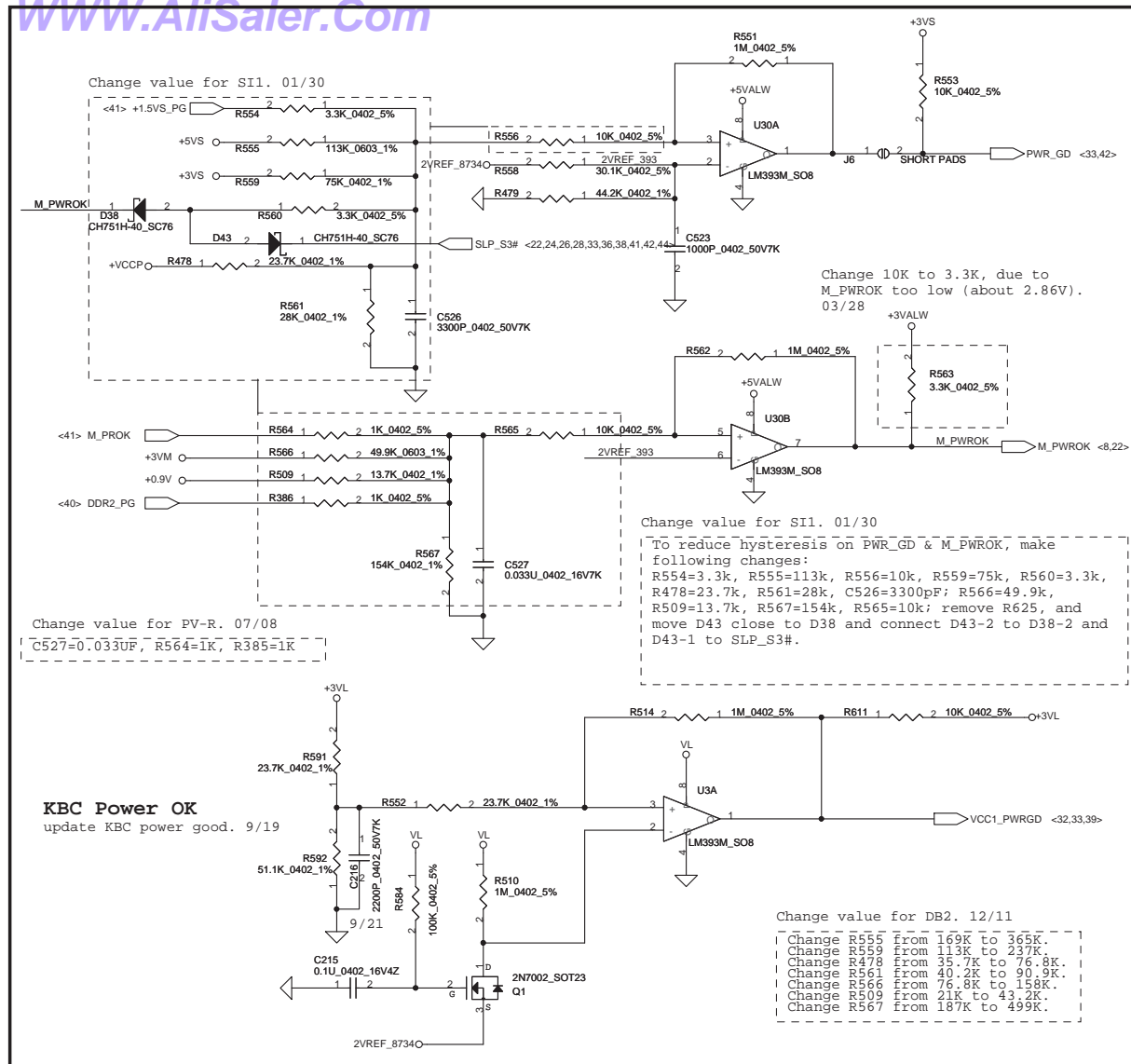


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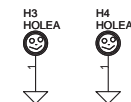




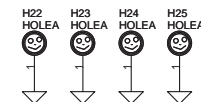
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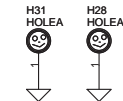
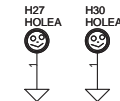
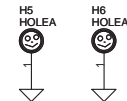
WWAN Card STANDOFF



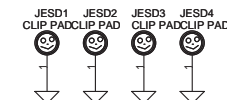
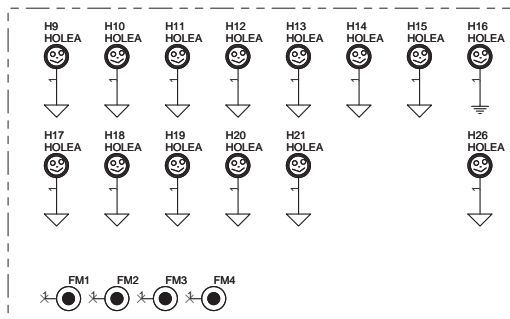
CPU support



MDC STANDOFF

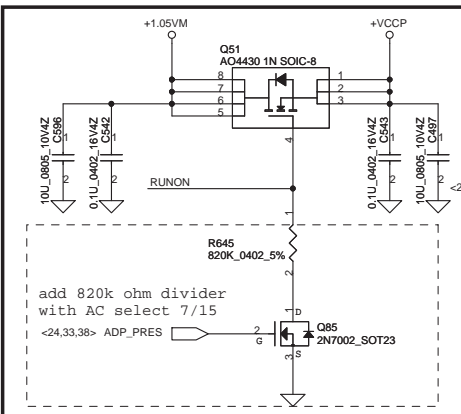


Del H1, H7 & H8. 1/18

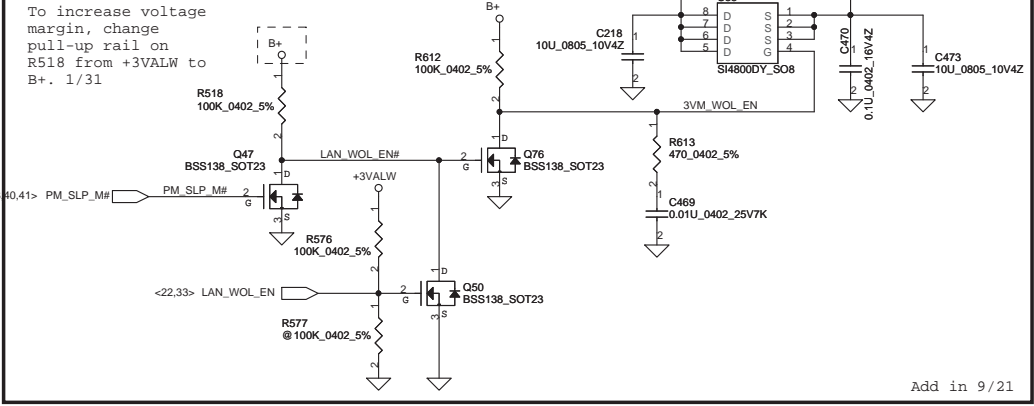


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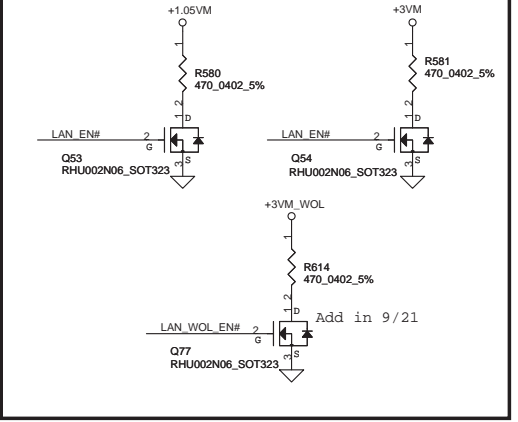
+1.05VM to +VCCP Transfer



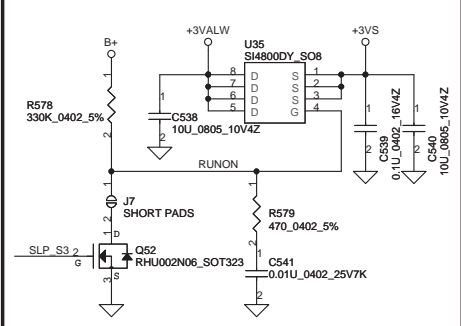
+3VALW to +3VM_WOL Transfer



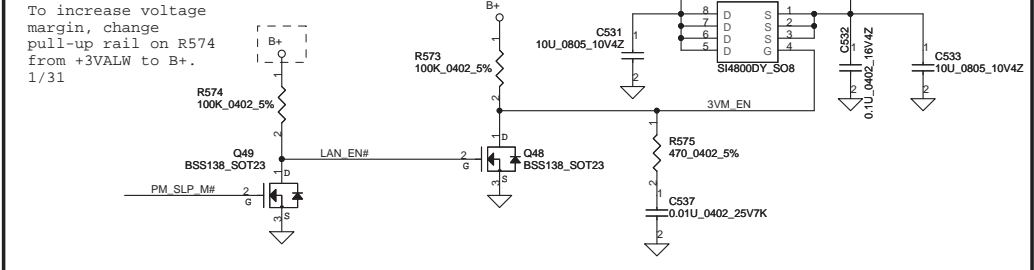
Discharge circuit-2 for V-M



+3VALW to +3VS Transfer

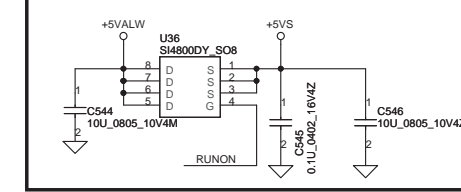


+3VALW to +3VM Transfer

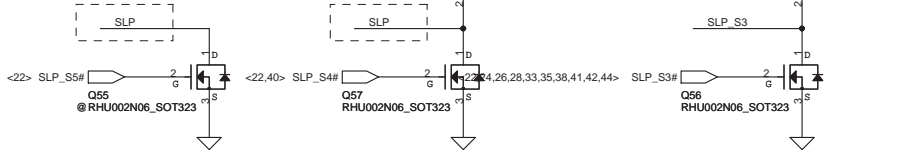


SYS. STATE	PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM
M-off / No WOL	0	0	0V	0V
M-off / WOL	0	1	3.3V	0V
M1 (ME on)	1	0	3.3V	3.3V
M1 (ME on)	1	1	3.3V	3.3V

+5VALW to +5VS Transfer



Design Change at 9/14.



Discharge circuit-1

